

CIRCUITS AND DEVICES: LABORATORY



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ENGR 261: Circuits Laboratory

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CHAPTER OVERVIEW

1: The Electrical Laboratory

Objective

The laboratory emphasizes the practical, hands-on component of this course. It complements the theoretical material presented in lecture, and as such, is integral and indispensable to the mastery of the subject. There are several items of importance here including proper safety procedures, required tools, and laboratory reports. This exercise will finish with an examination of scientific and engineering notation, the standard form of representing and manipulating values.

[1.1: Lab Safety and Tools](#)

[1.2: Laboratory Reports](#)

[1.3: Scientific and Engineering Notation](#)

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1.1: Lab Safety and Tools

If proper procedures are followed, the electrical lab is a perfectly safe place in which to work. There are some basic rules: No food or drink is allowed in lab at any time. Liquids are of particular danger as they are ordinarily conductive. While the circuitry used in lab is normally of no shock hazard, some of the test equipment may have very high internal voltages that could be lethal (in excess of 10,000 volts). Spilling a bottle of water or soda onto such equipment could leave the experimenter in the receiving end of a severe shock. Similarly, items such as books and jackets should not be left on top of the test equipment as it could cause overheating.

Each lab bench is self contained. All test equipment is arrayed along the top shelf. Beneath this shelf at the back of the work area is a power strip. All test equipment for this bench should be plugged into this strip. None of this equipment should be plugged into any other strip. This strip is controlled by a single circuit breaker which also controls the bench light. In the event of an emergency, all test equipment may be powered off through this one switch. Further, the benches are controlled by dedicated circuit breakers in the front of the lab. Next to this main power panel is an A/B/C class fire extinguisher suitable for electrical fires. Located at the rear of the lab is a safety kit. This contains bandages, cleaning swaps and the like for small cuts and the like. For serious injury, the Security Office will be contacted.

A lab bench should always be left in a secure mode. This means that the power to each piece of test equipment should be turned off, the bench itself should be turned off, all AC and DC power and signal sources should be turned down to zero, and all other equipment and components properly stowed with lab stools pushed under the bench.

It is important to come prepared to lab. This includes the class text, the lab exercise for that day, class notebook, calculator, and hand tools. The tools include an electronic breadboard, test leads, wire strippers, and needle-nose pliers or hemostats. A small pencil soldering iron may also be useful. A basic DMM (digital multimeter) rounds out the list.

A typical breadboard or protoboard is shown below:



Figure 1.1.1

This particular unit features two main wiring sections with a common strip section down the center. Boards can be larger or smaller than this and may or may not have the mounting plate as shown. The connections are spaced 0.1 inch apart which is the standard spacing for many semiconductor chips. These are clustered in groups of five common terminals to allow multiple connections. The exception is the common strip which may have dozens of connection points. These are called buses and are designed for power and ground connections. Interconnections are normally made using small diameter solid hookup wire, usually AWG 22 or 24. Larger gauges may damage the board while smaller gauges do not always make good connections and are easy to break.

In the picture below, the color highlighted sections indicate common connection points. Note the long blue section which is a bus. This unit has four discrete buses available. When building circuits on a breadboard, it is important to keep the interconnecting wires short and the layout as neat as possible. This will aid both circuit functioning and ease of troubleshooting.

Examples of breadboard usage can be found in Appendix D. Be sure to read it!

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1.2: Laboratory Reports

Unless specified otherwise, all lab exercises require a non-formal laboratory report. Lab reports are individual endeavors not group work. The deadline for reports is one week after the exercise is performed. A letter grade is subtracted for the first half-week late and two letter grades are subtracted for the second half-week late. Reports are not acceptable beyond one week late. A basic report should include a statement of the Objective (i.e., those items under investigation), a Conclusion (what was found or verified), a Discussion (an explanation and analysis of the lab data which links the Objective to the Conclusion), Data Tables and Graphs, and finally, answers to any problems or questions posed in the exercise. Details of the structure of the report along with an example report may be found in Appendices A, B and C.

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1.3: Scientific and Engineering Notation

Scientists and engineers often work with very large and very small numbers. The ordinary practice of using commas and leading zeroes proves to be very cumbersome in this situation. Scientific notation is more compact and less error prone method of representation. The number is split into two portions: a precision part (the mantissa) and a magnitude part (the exponent, being a power of ten). For example, the value 23,000 could be written as 23 times 10 to the 3rd power (that is, times one thousand). The exponent may be thought of in terms of how places the decimal point is moved to the left. Spelling this out is awkward, so a shorthand method is used where “times 10 to the X power” is replaced by the letter E (which stands for exponent). Thus, 23,000 could be written as 23E3. The value 45,000,000,000 would be written as 45E9. Note that it would also be possible to write this number as 4.5E10 or even 0.45E11. The only difference between scientific notation and engineering notation is that for engineering notation the exponent is always a multiple of three. Thus, 45E9 is proper engineering notation but 4.5E10 isn’t. On most scientific calculators E is represented by either an “EE” or “EXP” button. The process of entering the value 45E9 would be depressing the keys 4 5 EE 9.

For fractional values, the exponent is negative and may be thought of in terms how many places the decimal point must be moved to the right. Thus, 0.00067 may be written as 0.67E-3 or 6.7E-4 or even 670E-6. Note that only the first and last of these three are acceptable as engineering notation.

Engineering notation goes one step further by using a set of prefixes to replace the multiples of three for the exponent. The prefixes are:

E12 = Tera (T)	E9 = Giga (G)	E6 = Mega (M)	E3 = kilo (k)
E-3 = milli (m)	E-6 = micro (μ)	E-9 = nano (n)	E-12 = pico (p)

Table 1.3.1

Thus, 23,000 volts could be written as 23E3 volts or simply 23 kilovolts.

Besides being more compact, this notation is much simpler than the ordinary form when manipulating wide ranging values. When multiplying, simply multiply the precision portions and add the exponents. Similarly, when dividing, divide the precision portions and subtract the exponents. For example, 23,000 times 0.000003 may appear to be a complicated task. In engineering notation this is 23E3 times 3E-6. The result is 69E-3 (that is, 0.069). Given enough practice it will become second nature that kilo (E3) times micro (E-6) yields milli (E-3). This will facilitate lab estimates a great deal. Continuing, 42,000,000 divided by 0.002 is 42E6 divided by 2E-3, or 21E9 (the exponent is 6 minus a negative 3, or 9).

When adding or subtracting, first make sure that the exponents are the same (scaling if required) and then add or subtract the precision portions. For example, 2E3 plus 5E3 is 7E3. By comparison, 2E3 plus 5E6 is the same as 2E3 plus 5000E3, or 5002E3 (or 5.002E6).

Perform the following operations. Convert the following into scientific and engineering notation.

- 1,500
- 63,200,000
- 0.0234
- 0.000059
- 170

Convert the following into normal longhand notation:

- 1.23E3
- 54.7E6
- 2E-3
- 27E-9

10. $4.39\text{E}7$

Use the appropriate prefix for the following:

11. $4\text{E}6$ volts

12. $5.1\text{E}3$ feet

13. $3.3\text{E}-6$ grams

Perform the following operations:

14. $5.2\text{E}6 + 1.7\text{E}6$

15. $12\text{E}3 - 900$

16. $1.7\text{E}3 \cdot 2\text{E}6$

17. $48\text{E}3 / 4\text{E}6$

18. $20 / 4\text{E}3$

19. $10\text{ M} \cdot 2\text{ k}$

20. $8\text{ n} / 2\text{ m}$

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CHAPTER OVERVIEW

2: Sources and Instruments

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[2.1.1: Theory Overview](#)

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SECTION OVERVIEW

2.1: DC Sources and Metering

Objective

The objective of this exercise is to become familiar with the operation and usage of basic DC electrical laboratory devices, namely DC power supplies and digital multimeters.

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[2.1.2: Equipment](#)

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2.1.1: Theory Overview

The adjustable DC power supply is a mainstay of the electrical and electronics laboratory. It is indispensable in the prototyping of electronic circuits and extremely useful when examining the operation of DC systems. Of equal importance is the handheld digital multimeter or DMM. This device is designed to measure voltage, current, and resistance at a minimum, although some units may offer the ability to measure other parameters such as capacitance or transistor beta. Along with general familiarity of the operation of these devices, it is very important to keep in mind that no measurement device is perfect; their relative accuracy, precision, and resolution must be taken into account. Accuracy refers to how far a measurement is from that parameter's true value. Precision refers to the repeatability of the measurement, that is, the sort of variance (if any) that occurs when a parameter is measured several times. For a measurement to be valid, it must be both accurate and repeatable. Related to these characteristics is resolution. Resolution refers to the smallest change in measurement that may be discerned. For digital measurement devices this is ultimately limited by the number of significant digits available to display.

A typical DMM offers 3 1/2 digits of resolution, the half-digit referring to a leading digit that is limited to zero or one. This is also known as a "2000 count display", meaning that it can show a minimum of 0000 and a maximum of 1999. The decimal point is "floating" in that it could appear anywhere in the sequence. Thus, these 2000 counts could range from 0.000 volts up to 1.999 volts, or 00.00 volts to 19.99 volts, or 000.0 volts to 199.9 volts, and so forth. With this sort of limitation in mind, it is very important to set the DMM to the lowest range that won't produce an overload in order to achieve the greatest accuracy.

A typical accuracy specification would be 1% of the reading plus two counts. "Reading" refers to the value displayed. If the 2 volt range was selected to read 1 volt (a measurement range of 0.000 to 1.999 for a 3 1/2 digit meter), 1% would be 10 millivolts (0.01 volts). To this a further uncertainty of two counts (i.e., the finest digit) must be included. In this example, the finest digit is one millivolt (0.001 volts) so this adds another 2 millivolts for a total of 12 millivolts of potential inaccuracy. In other words, the value displayed by the meter could be as much as 12 millivolts higher or lower than the true value. For the 20 volt range the inaccuracy would be computed in like manner but notice that accuracy is lost because the lowest digit is larger (i.e., the "counts" represent a larger value). In this case, the counts portion jumps up to 20 mV for a total inaccuracy of 30 mV. Obviously, if a signal in the vicinity of, say, 1.3 volts was to be measured, greater accuracy will be obtained on the 2 volt scale than on either the 20 or 200 volt scales. In contrast, the 200 millivolt scale would produce an overload situation and cannot be used. Overloads are often indicated by either a flashing display or a readout of "OL". Finally, analog meters typically give a base accuracy in terms of a percentage of "full scale" (i.e., the selected scale or range) and not the signal itself, and obviously, there is no "counts" specification.

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2.1.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) Precision digital multimeter

model: _____ srn: _____

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2.1.3: Procedure

1. Assume a general purpose 3 1/2 digit DMM is being used. Its base accuracy is listed as 2% of reading plus 5 counts. Compute the inaccuracy caused by the scale and count factors and determine the total for a full scale reading. Record these values in Table 2.4.1.
 2. Repeat step one for a precision 4 1/2 digit DMM specified as 0.5% of reading plus 3 counts. Record the results in Table 2.4.2.
 3. Set the adjustable power supply to 2.2 volts via its display. Use both the Coarse and Fine controls to get as close to 2.2 volts as possible. Record the displayed voltage in the first column of Table 2.4.3. Using the general purpose DMM set to the DC voltage function, set the range to 20 volts full scale. Measure the voltage at the output jacks of the power supply. Be sure to connect the DMM and power supply red lead to red lead, and black lead to black lead. Record the voltage registered by the DMM in the middle column of Table 2.4.3. Reset the DMM to the 200 volt scale, re-measure the voltage, and record in the final column
 4. Repeat step three for the remaining voltages of Table 2.4.3.
 5. Using the precision DMM, repeat steps three and four, recording the results in Table 2.4.4.
-

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2.1.4: Data Tables

Scale	2% Reading	5 Counts	Total
200 mV			
20 V			

Table 2.1.4.1

Scale	.5% Reading	3 Counts	Total
200 mV			
20 V			

Table 2.1.4.2

Voltage	Power Supply	DMM 20V Scale	DMM 200V Scale
2.2			
5.0			
9.65			
15.0			

Table 2.1.4.3

Voltage	Power Supply	DMM 20V Scale	DMM 200V Scale
2.2			
5.0			
9.65			
15.0			

Table 2.1.4.4

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2.1.5: Questions

1. For the general purpose DMM of Table 2.4.1, which contributes the larger share of inaccuracy; the full scale percentage or the count spec?
 2. Bearing in mind that the power supply display is really just a very limited sort of digital volt meter, which voltages in Table 2.4.3 and 2.4.4 do you suspect to be the most accurately measured and why?
 3. Assuming that the precision DMM used in Table 2.4.4 has a base accuracy spec of 0.1% plus 2 counts and is properly calibrated, what is the range of possible “true” voltages measured for 15.0 volts on the 20 volt scale?
-

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SECTION OVERVIEW

3.1: Resistor Color Code

Objective

The objective of this exercise is to become familiar with the measurement of resistance values using a digital multimeter (DMM). A second objective is to learn the resistor color code.

[3.1.1: Theory Overview](#)

[3.1.2: Equipment](#)

[3.1.3: Procedure](#)

[3.1.4: Data Tables](#)

[3.1.5: Questions](#)

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3.1.1: Theory Overview

The resistor is perhaps the most fundamental of all electrical devices. Its fundamental attribute is the restriction of electrical current flow: The greater the resistance, the greater the restriction of current. Resistance is measured in ohms. The measurement of resistance in unpowered circuits may be performed with a digital multimeter. Like all components, resistors cannot be manufactured to perfection. That is, there will always be some variance of the true value of the component when compared to its nameplate or nominal value. For precision resistors, typically 1% tolerance or better, the nominal value is usually printed directly on the component. Normally, general purpose components, i.e. those worse than 1%, usually use a color code to indicate their value.

The resistor color code typically uses 4 color bands. The first two bands indicate the precision values (i.e. the mantissa) while the third band indicates the power of ten applied (i.e. the number of zeroes to add). The fourth band indicates the tolerance. It is possible to find resistors with five or six bands but they will not be examined in this exercise. Examples are shown below:

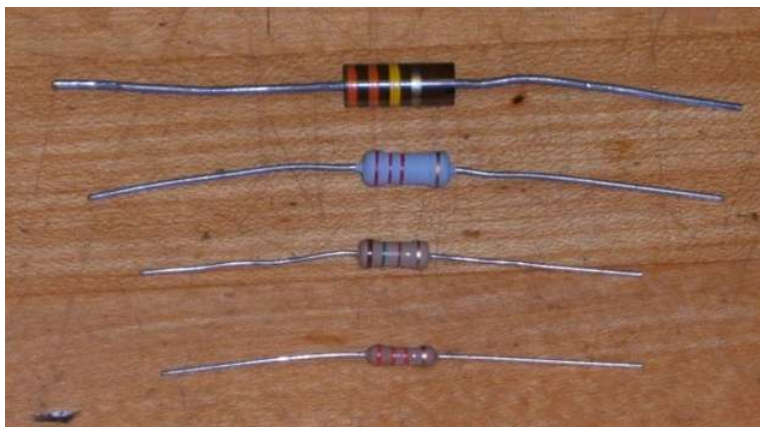


Figure 3.1.1.1

It is important to note that the physical size of the resistor indicates its power dissipation rating, not its ohmic value.

Each color in the code represents a numeral. It starts with black and finishes with white, going through the rainbow in between:

0 Black	1 Brown	2 Red	3 Orange	4 Yellow
5 Green	6 Blue	7 Violet	8 Gray	9 White

Table 3.1.1.1

For the fourth, or tolerance, band:

5% Gold	10% Silver	20% None
---------	------------	----------

Table 3.1.1.2

For example, a resistor with the color code brown-red-orange-silver would correspond to 12 followed by 3 zeroes, or 12,000 ohms (more conveniently, 12 k ohms). It would have a tolerance of 10% of 12 k ohms or 1200 ohms. This means that the actual value of any particular resistor with this code could be anywhere between $12,000 - 1200 = 10,800$, to $12,000 + 1200 = 13,200$. That is, 10.8 k to 13.2 k ohms. Note, the IEC standard replaces the decimal point with the engineering prefix, thus 1.2 k is alternately written 1k2.

Similarly, a 470 k 5% resistor would have the color code yellow-violet-yellow-gold. To help remember the color code many mnemonics have been created using the first letter of the colors to create a sentence. One example is the picnic mnemonic Black Bears Robbed Our Yummy Goodies Beating Various Gray Wolves.

Measurement of resistors with a DMM is a very straight forward process. Simply set the DMM to the resistance function and choose the first scale that is higher than the expected value. Clip the leads to the resistor and record the resulting value.

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3.1.2: Equipment

(1) Digital multimeter

model: _____ srn: _____

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3.1.3: Procedure

1. Given the nominal values and tolerances in Table 3.4.1, determine and record the corresponding color code bands.
 2. Given the color codes in Table 3.4.2, determine and record the nominal value, tolerance and the minimum and maximum acceptable values.
 3. Obtain a resistor equal to the first value listed in Table 3.4.3. Determine the minimum and maximum acceptable values based on the nominal value and tolerance. Record these values in Table 3.4.3. Using the DMM, measured the actual value of the resistor and record it in Table 3.4.3. Determine the deviation percentage of this component and record it in Table 3.4.3. The deviation percentage may be found via: $\text{Deviation} = 100 * (\text{measured} - \text{nominal})/\text{nominal}$. Circle the deviation if the resistor is out of tolerance.
 4. Repeat Step 3 for the remaining resistor in Table 3.4.3.
-

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3.1.4: Data Tables

Value	Band 1	Band 2	Band 3	Band 4
27 @ 10%				
56 @ 10%				
180 @ 5%				
390 @ 10%				
680 @ 5%				
1.5 k @ 20%				
3.6 k @ 10%				
7.5 k @ 5%				
10 k @ 5%				
47 k @ 10%				
820 k @ 10%				
2.2 M @ 20 %				

Table 3.1.4.1

Colors	Nominal	Tolerance	Minimum	Maximum
red-red-black-silver				
blue-gray-black-gold				
brown-green-brown-gold				
orange-orange-brown-silver				
green-blue-brown –gold				
brown-red-red–silver				
red-violet-red–silve				
gray-red-red–gold				
brown-black-orange–gold				
orange-orange-orange–silver				
blue-gray-yellow–none				
green-black-green-silver				

Table 3.1.4.2

Value	Minimum	Maximum	Measured	Deviation
22 @ 10%				
68 @ 5%				
150 @ 5%				
330 @ 10%				
560 @ 5%				
1.2 k @ 5%				
2.7 k @ 10%				
8.2 k @ 5%				
10 k @ 5%				
33 k @ 10%				
680 k @ 10%				
5 M @ 20 %				

Table 3.1.4.3

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3.1.5: Questions

1. What is the largest deviation in Table 3.4.3? Would it ever be possible to find a value that is outside the stated tolerance? Why or why not?
 2. If Steps 3 and 4 were to be repeated with another batch of resistors, would the final two columns be identical to the original Table 3.4.3? Why or why not?
 3. Do the measured values of Table 3.4.3 represent the exact values of the resistors tested? Why or why not?
-

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SECTION OVERVIEW

3.2: Ohm's Law

Objective

This exercise examines Ohm's law, one of the fundamental laws governing electrical circuits. It states that voltage is equal to the product of current times resistance.

[3.2.1: Theory Overview](#)

[3.2.2: Equipment](#)

[3.2.3: Schematic](#)

[3.2.4: Procedure](#)

[3.2.5: Data Tables](#)

[3.2.6: Questions](#)

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3.2.1: Theory Overview

Ohm's law is commonly written as $V = I * R$. That is, for a given current, an increase in resistance will result in a greater voltage. Alternately, for a given voltage, an increase in resistance will produce a decrease in current. As this is a first order linear equation, plotting current versus voltage for a fixed resistance will yield a straight line. The slope of this line is the conductance, and conductance is the reciprocal of resistance. Therefore, for a high resistance, the plot line will appear closer to the horizontal while a lower resistance will produce a more vertical plot line.

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3.2.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 1 k Ω resistor

(1) 6.8 k Ω resistor

(1) 33 k Ω resistor

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3.2.3: Schematic

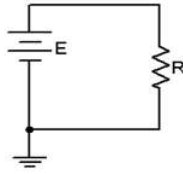


Figure 3.2.3.1

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3.2.4: Procedure

1. Build the circuit of Figure 4.1 using the 1 k Ω resistor. Set the DMM to measure DC current and insert it in-line between the source and resistor. Set the source for zero volts. Measure and record the current in Table 4.5.1. Note that the theoretical current is 0 and any measured value other than 0 would produce an undefined percent deviation.
 2. Setting E at 2 volts, determine the theoretical current based on Ohm's law and record this in Table 4.5.1. Measure the actual current, determine the deviation, and record these in Table 4.5.1. Note that $\text{Deviation} = 100 * (\text{measured} - \text{theory}) / \text{theory}$.
 3. Repeat step 2 for the remaining source voltages in Table 4.5.1.
 4. Remove the 1 k Ω and replace it with the 6.8 k Ω . Repeat steps 1 through 3 using Table 4.5.2.
 5. Remove the 6.8 k Ω and replace it with the 33 k Ω . Repeat steps 1 through 3 using Table 4.5.3.
 6. Using the measured currents from Tables 4.5.1, 4.5.2, and 4.5.3, create a plot of current versus voltage. Plot all three curves on the same graph. Voltage is the horizontal axis and current is the vertical axis.
-

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3.2.5: Data Tables

E (volts)	I theory	I measured	Deviation
0	0		
2			
4			
6			
8			
10			
12			

Table 3.2.5.1 (1 k Ω)

E (volts)	I theory	I measured	Deviation
0	0		
2			
4			
6			
8			
10			
12			

Table 3.2.5.1 (6.8 k Ω)

E (volts)	I theory	I measured	Deviation
0	0		
2			
4			
6			
8			
10			
12			

Table 3.2.5.1 (33 k Ω)

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3.2.6: Questions

1. Does Ohm's law appear to hold in this exercise?
 2. Is there a linear relationship between current and voltage?
 3. What is the relationship between the slope of the plot line and the circuit resistance?
-

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SECTION OVERVIEW

3.3: Potentiometers and Rheostats

Objectives

The objective of this exercise is to examine the practical workings of adjustable resistances, namely the potentiometer and rheostat. Their usage in adjustable voltage and current control will be investigated.

[3.3.1: Theory Overview](#)

[3.3.2: Equipment](#)

[3.3.3: Schematics](#)

[3.3.4: Procedure](#)

[3.3.5: Data Tables](#)

[3.3.6: Questions](#)

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3.3.1: Theory Overview

A potentiometer is a three terminal resistive device. The outer terminals present a constant resistance which is the nominal value of the device. A third terminal, called the wiper arm, is in essence a contact point that can be moved along the resistance. Thus, the resistance seen from one outer terminal to the wiper plus the resistance from the wiper to the other outer terminal will always equal the nominal resistance of the device. This three terminal configuration is used typically to adjust voltage via the voltage divider rule, hence the name potentiometer, or pot for short. While the resistance change is often linear with rotation (i.e., rotating the shaft 50% yields 50% resistance), other schemes, called tapers, are also found. One common non-linear taper is the logarithmic taper. It is important to note that linearity can be compromised (sometimes on purpose) if the resistance loading the potentiometer is not significantly larger in value than the potentiometer itself.

If only a single outer terminal and the wiper are used, the device is merely an adjustable resistor and is referred to as a rheostat. These may be placed in-line with a load to control the load current, the greater the resistance, the smaller the current.

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3.3.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 10 k Ω potentiometer

(1) 100 k Ω potentiometer

(1) 1 k Ω

(1) 4.7 k Ω

(1) 47 k Ω

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3.3.3: Schematics

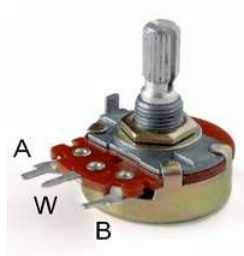


Figure 3.3.3.1

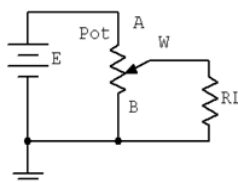


Figure 3.3.3.2

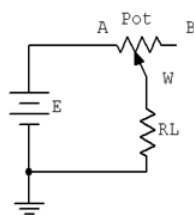


Figure 3.3.3.3

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3.3.4: Procedure

1. A typical potentiometer is shown in Figure 9.3.1. Using a 10 k pot, first rotate the knob fully counterclockwise and using the DMM, measure the resistance from terminal A to the wiper arm, W. Then measure the value from the wiper arm to terminal B. Record these values in Table 9.5.1. Add the two readings, placing the result in the final column.
2. Rotate the knob 1/4 turn clockwise and repeat the measurements of step 1. Repeat this process for the remaining knob positions in Table 9.5.1. Note that the results of the final column should all equal the nominal value of the potentiometer.
3. Construct the circuit of Figure 9.3.2 using $E = 10$ volts, a 10 k potentiometer and leave R_L open. Rotate the knob fully counterclockwise and measure the voltage from the wiper to ground. Record this value in Table 9.5.2. Continue taking and recording voltages as the knob is rotated to the other four positions in Table 9.5.2.
4. Set R_L to 47 k and repeat step 3.
5. Set R_L to 4.7 k and repeat step 3.
6. Set R_L to 1 k and repeat step 3.
7. Using a linear grid, plot the voltages of Table 9.5.2 versus position. Note that there will be four curves created, one for each load, but place them on a single graph. Note how the variance of the load affects the linearity and control of the voltage.
8. Construct the circuit of Figure 9.3.3 using $E = 10$ volts, a 100 k potentiometer and $R_L = 1$ k. Rotate the knob fully counterclockwise and measure the current through the load. Record this value in Table 9.5.3. Repeat this process for the remaining knob positions in Table 9.5.3.
9. Replace the load resistor with a 4.7 k and repeat step 8.

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3.3.5: Data Tables

Position	R_{AW}	R_{WB}	$R_{AW} + R_{WB}$
Fully CCW			
1/4			
1/2			
3/4			
Fully CW			

Table 3.3.5.1

Position	V_{WB} Open	V_{WB} 47k	V_{WB} 4.7k	V_{WB} 1k
Fully CCW				
1/4				
1/2				
3/4				
Fully CW				

Table 3.3.5.2

Position	I_L 1k	I_L 4.7k
Fully CCW		
1/4		
1/2		
3/4		
Fully CW		

Table 3.3.5.3

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3.3.6: Questions

1. In Table 9.5.1, does the total resistance always equal the nominal resistance of the potentiometer?
 2. If the potentiometer used for Table 9.5.1 had a logarithmic taper, how would the values change?
 3. In Table 9.5.2, is the load voltage always directly proportional to the knob position? Is the progression always linear?
 4. Explain the variation of the four curves plotted in step 7.
 5. In the final circuit, is the load current always proportional to the knob position? If the load was much smaller, say just a few hundred ohms, would the minimum and maximum currents be much different from those in Table 9.5.3?
 6. How could the circuit of Figure 9.3.3 be modified so that the maximum current could be set to a value higher than that achieved by the supply and load resistor alone?
-

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SECTION OVERVIEW

3.4: Series DC Circuits

Objective

The focus of this exercise is an examination of basic series DC circuits with resistors. A key element is Kirchhoff's voltage law which states that the sum of voltage rises around a loop must equal the sum of the voltage drops. The voltage divider rule will also be investigated.

[3.4.1: Theory Overview](#)

[3.4.2: Equipment](#)

[3.4.3: Schematics](#)

[3.4.4: Procedure](#)

[3.4.5: Data Tables](#)

[3.4.6: Questions](#)

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3.4.1: Theory Overview

A series circuit is defined by a single loop in which all components are arranged in daisy-chain fashion. The current is the same at all points in the loop and may be found by dividing the total voltage source by the total resistance. The voltage drops across any resistor may then be found by multiplying that current by the resistor value. Consequently, the voltage drops in a series circuit are directly proportional to the resistance. An alternate technique to find the voltage is the voltage divider rule. This states that the voltage across any resistor (or combination of resistors) is equal to the total voltage source times the ratio of the resistance of interest to the total resistance.

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3.4.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 1 k Ω

(1) 2.2 k Ω

(1) 3.3 k Ω

(1) 6.8 k Ω

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3.4.3: Schematics

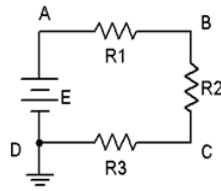


Figure 3.4.3.1

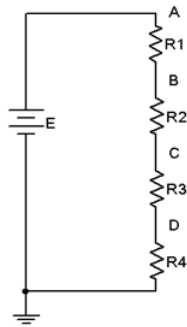


Figure 3.4.3.2

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3.4.4: Procedure

1. Using the circuit of Figure 5.3.1 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 3.3\text{ k}$, and $E = 10\text{ volts}$, determine the theoretical current and record it in Table 5.5.1. Construct the circuit. Set the DMM to read DC current and insert it in the circuit at point A. Remember, ammeters go in-line and require the circuit to be opened for proper measurement. The red lead should be placed closer to the positive source terminal. Record this current in Table 5.5.1. Repeat the current measurements at points B and C.
2. Using the theoretical current found in Step 1, apply Ohm's law to determine the expected voltage drops across R_1 , R_2 , and R_3 . Record these values in the Theory column of Table 5.5.2.
3. Set the DMM to measure DC voltage. Remember, unlike current, voltage is measured across components. Place the DMM probes across R_1 and measure its voltage. Again, red lead should be placed closer to the positive source terminal. Record this value in Table 5.5.2. Repeat this process for the voltages across R_2 and R_3 . Determine the percent deviation between theoretical and measured for each of the three resistor voltages and record these in the final column of Table 5.5.2.
4. Consider the circuit of Figure 5.3.2 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 3.3\text{ k}$, $R_4 = 6.8\text{ k}$ and $E = 20\text{ volts}$. Using the voltage divider rule, determine the voltage drops across each of the four resistors and record the values in Table 5.5.3 under the Theory column. Note that the larger the resistor, the greater the voltage should be. Also determine the potentials V_{AC} and V_B , again using the voltage divider rule.
5. Construct the circuit of Figure 5.3.2 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 3.3\text{ k}$, $R_4 = 6.8\text{ k}$ and $E = 20\text{ volts}$. Set the DMM to measure DC voltage. Place the DMM probes across R_1 and measure its voltage. Record this value in Table 5.5.3. Also determine the deviation. Repeat this process for the remaining three resistors.
6. To find V_{AC} , place the red probe on point A and the black probe on point C. Similarly, to find V_B , place the red probe on point B and the black probe on ground. Record these values in Table 5.5.3 with deviations.

5.4.1: Simulation

7. Build the circuit of Figure 5.3.1 in a simulator. Using the virtual DMM as a voltmeter determine the voltages at nodes A, B and C, and compare these to the theoretical and measured values recorded in Table 5.5.2.

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3.4.5: Data Tables

I Theory	I Point A	I Point B	I Point C

Table 3.4.5.1

Voltage	Theory	Measured	Deviation
R1			
R2			
R3			

Table 3.4.5.2

Voltage	Theory	Measured	Deviation
R1			
R2			
R3			
R4			
V_{AC}			
V_B			

Table 3.4.5.3

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3.4.6: Questions

1. For the circuit of Figure 5.3.1, what is the expected current measurement at point D?
 2. For the circuit of Figure 5.3.2, what are the expected current and voltage measurements at point D?
 3. In Figure 5.3.2, R4 is approximately twice the size of R3 and about three times the size of R2. Would the voltages exhibit the same ratios? Why/why not? What about the currents through the resistors?
 4. If a fifth resistor of 10 k Ω was added below R4 in Figure 5.3.2, how would this alter V_{AC} and V_B ? Show work.
 5. Is KVL satisfied in Tables 5.5.2 and 5.5.3?
-

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SECTION OVERVIEW

3.5: Parallel DC Circuits

Objective

The focus of this exercise is an examination of basic parallel DC circuits with resistors. A key element is Kirchhoff's current law which states that the sum of currents entering a node must equal the sum of the currents exiting that node. The current divider rule will also be investigated.

[3.5.1: Theory Overview](#)

[3.5.2: Equipment](#)

[3.5.3: Schematics](#)

[3.5.4: Procedure](#)

[3.5.5: Data Tables](#)

[3.5.6: Questions](#)

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3.5.1: Theory Overview

A parallel circuit is defined by the fact that all components share two common nodes. The voltage is the same across all components and will equal the applied source voltage. The total supplied current may be found by dividing the voltage source by the equivalent parallel resistance. It may also be found by summing the currents in all of the branches. The current through any resistor branch may be found by dividing the source voltage by the resistor value. Consequently, the currents in a parallel circuit are inversely proportional to the associated resistances. An alternate technique to find a particular current is the current divider rule. For a two resistor circuit this states that the current through one resistor is equal to the total current times the ratio of the other resistor to the total resistance.

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3.5.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 1 k Ω

(1) 2.2 k Ω

(1) 3.3 k Ω

(1) 6.8 k Ω

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3.5.3: Schematics

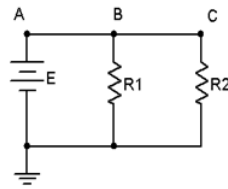


Figure 3.5.3.1

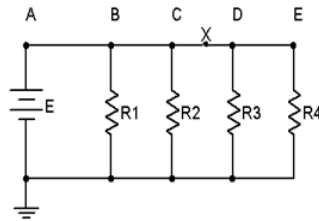


Figure 3.5.3.2

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3.5.4: Procedure

1. Using the circuit of Figure 6.3.1 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$ and $E = 8\text{ volts}$, determine the theoretical voltages at points A, B, and C with respect to ground. Record these values in Table 6.5.1. Construct the circuit. Set the DMM to read DC voltage and apply it to the circuit from point A to ground. The red lead should be placed at point A and the black lead should be connected to ground. Record this voltage in Table 6.5.1. Repeat the measurements at points B and C.
2. Apply Ohm's law to determine the expected currents through R_1 and R_2 . Record these values in the Theory column of Table 6.5.2. Also determine and record the total current.
3. Set the DMM to measure DC current. Remember, current is measured at a single point and requires the meter to be inserted in-line. To measure the total supplied current place the DMM between points A and B. The red lead should be placed closer to the positive source terminal. Record this value in Table 6.5.2. Repeat this process for the currents through R_1 and R_2 . Determine the percent deviation between theoretical and measured for each of the currents and record these in the final column of Table 6.5.2.
4. Crosscheck the theoretical results by computing the two resistor currents through the current divider rule. Record these in Table 6.5.3.
5. Consider the circuit of Figure 6.3.2 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 3.3\text{ k}$, $R_4 = 6.8\text{ k}$ and $E = 10\text{ volts}$. Using the Ohm's law, determine the currents through each of the four resistors and record the values in Table 6.5.4 under the Theory column. Note that the larger the resistor, the smaller the current should be. Also determine and record the total supplied current and the current I_X . Note that this current should equal the sum of the currents through R_3 and R_4 .
6. Construct the circuit of Figure 6.3.2 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 3.3\text{ k}$, $R_4 = 6.8\text{ k}$ and $E = 10\text{ volts}$. Set the DMM to measure DC current. Place the DMM probes in-line with R_1 and measure its current. Record this value in Table 6.5.4. Also determine the deviation. Repeat this process for the remaining three resistors. Also measure the total current supplied by the source by inserting the ammeter between points A and B.
7. To find I_X , insert the ammeter at point X with the black probe closer to R_3 . Record this value in Table 6.5.4 with deviation.

6.4.1: Simulation

8. Build the circuit of Figure 6.3.2 in a simulator. Using the virtual DMM as an ammeter determine the currents through the four resistors along with I_X , and compare these to the theoretical and measured values recorded in Table 6.5.4.

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3.5.5: Data Tables

Voltage	Theory	Measured
V_A		
V_B		
V_C		

Table 3.5.5.1

Current	Theory	Measured	Deviation
R1			
R2			
Total			

Table 3.5.5.2

Current	CDR Theory
R1	
R2	
Total	

Table 3.5.5.3

Current	Theory	Measured	Deviation
R1			
R2			
R3			
R4			
Total			
I_X			

Table 3.5.5.4

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3.5.6: Questions

1. For the circuit of Figure 6.3.1, what is the expected current entering the negative terminal of the source?
 2. For the circuit of Figure 6.3.2, what is the expected current between points B and C?
 3. In Figure 6.3.2, R4 is approximately twice the size of R3 and about three times the size of R2. Would the currents exhibit the same ratios? Why/why not?
 4. If a fifth resistor of 10 k Ω was added to the right of R4 in Figure 6.3.2, how would this alter I_{Total} and I_X ? Show work.
 5. Is KCL satisfied in Tables 6.5.2 and 6.5.4?
-

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SECTION OVERVIEW

3.6: Series-Parallel DC Circuits

Objective

This exercise will involve the analysis of basic series-parallel DC circuits with resistors. The use of simple series-only and parallel-only sub-circuits is examined as one technique to solve for desired currents and voltages.

[3.6.1: Theory Overview](#)

[3.6.2: Equipment](#)

[3.6.3: Schematics](#)

[3.6.4: Procedure](#)

[3.6.5: Data Tables](#)

[3.6.6: Questions](#)

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3.6.1: Theory Overview

Simple series-parallel networks may be viewed as interconnected series and parallel sub-networks. Each of these sub-networks may be analyzed through basic series and parallel techniques such as the application of voltage divider and current divider rules along with Kirchhoff's voltage and current laws. It is important to identify the most simple series and parallel connections in order to jump to more complex interconnections.

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3.6.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 1 k Ω

(1) 2.2 k Ω

(1) 3.3 k Ω

(1) 4.7 k Ω

(1) 6.8 k Ω

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3.6.3: Schematics

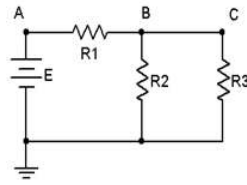


Figure 3.6.3.1

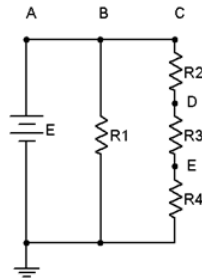


Figure 3.6.3.2

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3.6.4: Procedure

1. Consider the circuit of Figure 7.3.1 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 4.7\text{ k}$ and $E = 10\text{ volts}$. R_2 is in parallel with R_3 . This combination is in series with R_1 . Therefore, the R_2, R_3 pair may be treated as a single resistance to form a series loop with R_1 . Based on this observation, determine the theoretical voltages at points A, B, and C with respect to ground. Record these values in Table 7.5.1. Construct the circuit. Set the DMM to read DC voltage and apply it to the circuit from point A to ground. Record this voltage in Table 7.5.1. Repeat the measurements at points B and C, determine the deviations, and record the values in Table 7.5.1.
2. Applying KCL to the parallel sub-network, the current entering node B (i.e., the current through R_1) should equal the sum of the currents flowing through R_2 and R_3 . These currents may be determined through Ohm's law and/or the current divider rule. Compute these currents and record them in Table 7.5.2. Using the DMM as an ammeter, measure these three currents and record the values along with deviations in Table 7.5.2.
3. Consider the circuit of Figure 7.3.2. R_2, R_3 and R_4 create a series sub-network. This sub-network is in parallel with R_1 . By observation then, the voltages at nodes A, B and C should be identical as in any parallel circuit of similar construction. Due to the series connection, the same current flows through R_2, R_3 and R_4 . Further, the voltages across R_2, R_3 and R_4 should sum up to the voltage at node C, as in any similarly constructed series network. Finally, via KCL, the current exiting the source must equal the sum of the currents entering R_1 and R_2 .
4. Build the circuit of Figure 7.3.2 with $R_1 = 3.3\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 4.7\text{ k}$, $R_4 = 6.8\text{ k}$ and $E = 20\text{ volts}$. Using the series and parallel relations noted in Step 3, calculate the voltages at points B, C, D and E. Measure these potentials with the DMM, determine the deviations, and record the values in Table 7.5.3.
5. Calculate the currents leaving the source and flowing through R_1 and R_2 . Record these values in Table 7.5.4. Using the DMM as an ammeter, measure those same currents, compute the deviations, and record the results in Table 7.5.4.

7.4.1: Simulation

6. Build the circuit of Figure 7.3.1 in a simulator. Using the virtual DMM as a voltmeter determine the voltages at nodes A, B and C, and compare these to the theoretical and measured values recorded in Table 7.5.1.
7. Build the circuit of Figure 7.3.2 in a simulator. Using the DC Operating Point simulation function, determine the voltages at nodes B, C, D and E, and compare these to the theoretical and measured values recorded in Table 7.5.3.

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3.6.5: Data Tables

Voltage	Theory	Measured	Deviation
V_A			
V_B			
V_C			

Table 3.6.5.1

Current	Theory	Measured	Deviation
R_1			
R_2			
R_3			

Table 3.6.5.2

Voltage	Theory	Measured	Deviation
V_B			
V_C			
V_D			
V_E			

Table 3.6.5.3

Current	Theory	Measured	Deviation
Source			
R_1			
R_2			

Table 3.6.5.4

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3.6.6: Questions

1. Are KVL and KCL satisfied in Tables 7.5.1 and 7.5.2?
 2. Are KVL and KCL satisfied in Tables 7.5.3 and 7.5.4?
 3. How would the voltages at A and B in Figure 7.3.1 change if a fourth resistor equal to 10 k was added in parallel with R3? What if this resistor was added in series with R3?
 4. How would the currents through R1 and R2 in Figure 7.3.2 change if a fifth resistor equal to 10 k was added in series with R1? What if this resistor was added in parallel with R1?
-

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SECTION OVERVIEW

3.7: Ladders and Bridges

Objective

The objective of this exercise is to continue the exploration of basic series-parallel DC circuits. The basic ladder network and bridge are examined. A key element here is the concept of loading, that is, the effect that a sub-circuit may have on a neighboring sub-circuit.

[3.7.1: Theory Overview](#)

[3.7.2: Equipment](#)

[3.7.3: Schematics](#)

[3.7.4: Procedure](#)

[3.7.5: Data Tables](#)

[3.7.6: Questions](#)

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3.7.1: Theory Overview

Ladder networks are comprised of a series of alternating series and parallel connections. Each section effectively loads the prior section, meaning that the voltage and current of the prior section may change considerably if the loading section is removed. One possible technique for the solution of ladder networks is a series of cascading voltage dividers. Current dividers may also be used. In contrast, bridge networks typically make use of four elements arranged in dual series and parallel configuration. These are often used in measurement systems with the voltage of interest derived from the difference of two series subcircuit voltages. As in the simpler series-parallel networks; KVL, KCL, the current divider rule and the voltage divider rule may be used in combination to analyze the sub-circuits.

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3.7.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 1 k Ω

(1) 2.2 k Ω

(1) 3.3 k Ω

(1) 6.8 k Ω

(1) 10 k Ω

(1) 22 k Ω

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3.7.3: Schematics

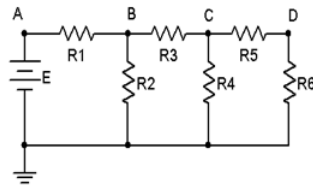


Figure 3.7.3.1

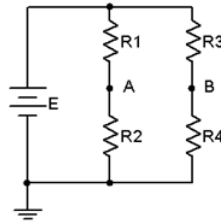


Figure 3.7.3.2

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3.7.4: Procedure

1. Consider the circuit of Figure 8.3.1. R5 and R6 form a simple series connection. Together, they are in parallel with R4. Therefore the voltage across R4 must be the same as the sum of the voltages across R5 and R6. Similarly, the current entering node C from R3 must equal the sum of the currents flowing through R4 and R5. This three resistor combination is in series with R3 in much the same manner than R6 is in series with R5. These four resistors are in parallel with R2, and finally, these five resistors are in series with R1. Note that to find the voltage at node B the voltage divider rule may be used, however, it is important to note that VDR cannot be used in terms of R1 versus R2. Instead, R1 reacts against the entire series-parallel combination of R2 through R6. Similarly, R3 reacts against the combination of R4, R5 and R6. That is to say R5 and R6 load R4, and R3 through R6 load R2. Because of this process note that V_D must be less than V_C , which must be less than V_B , which must be less than V_A . Thus the circuit may be viewed as a sequence of loaded voltage dividers.
2. Construct the circuit of Figure 8.3.1 using $R1 = 1\text{ k}$, $R2 = 2.2\text{ k}$, $R3 = 3.3\text{ k}$, $R4 = 6.8\text{ k}$, $R5 = 10\text{ k}$, $R6 = 22\text{ k}$ and $E = 20\text{ volts}$. Based on the observations of Step 1, determine the theoretical voltages at nodes A, B, C and D, and record them in Table 8.5.1. Measure the potentials with a DMM, compute the deviations and record the results in Table 8.5.1.
3. Based on the theoretical voltages found in Table 8.5.1, determine the currents through R1, R2, R4 and R6. Record these values in Table 8.5.2. Measure the currents with a DMM, compute the deviations and record the results in Table 8.5.2.
4. Consider the circuit of Figure 8.3.2. In this bridge network, the voltage of interest is V_{AB} . This may be directly computed from $V_A - V_B$. Assemble the circuit using $R1 = 1\text{ k}$, $R2 = 2.2\text{ k}$, $R3 = 10\text{ k}$, $R4 = 6.8\text{ k}$ and $E = 10\text{ volts}$. Determine the theoretical values for V_A , V_B and V_{AB} and record them in Table 8.5.3. Note that the voltage divider rule is very effective here as the R1 R2 branch and the R3 R4 branch are in parallel and therefore both “see” the source voltage.
5. Use the DMM to measure the potentials at A and B with respect to ground, the red lead going to the point of interest and the black lead going to ground. To measure the voltage from A to B, the red lead is connected to point A while the black is connected to point B. Record these potentials in Table 8.5.3. Determine the deviations and record these in Table 8.5.3.

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3.7.5: Data Tables

Voltage	Theory	Measured	Deviation
V_A			
V_B			
V_C			
V_D			

Table 3.7.5.1

Current	Theory	Measured	Deviation
R_1			
R_2			
R_4			
R_6			

Table 3.7.5.2

Voltage	Theory	Measured	Deviation
V_A			
V_B			
V_{AB}			

Table 3.7.5.3

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3.7.6: Questions

1. In Figure 8.3.1, if another pair of resistors was added across R6, would V_D go up, down, or stay the same? Why?
 2. In Figure 8.3.1, if R4 was accidentally opened would this change the potentials at B, C and D? Why or why not?
 3. If the DMM leads are reversed in Step 5, what happens to the measurements in Table 8.5.3?
 4. Suppose that R3 and R4 are accidentally swapped in Figure 8.3.2. What is the new V_{AB} ?
-

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CHAPTER OVERVIEW

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SECTION OVERVIEW

4.1: Superposition Theorem

Objective

The objective of this exercise is to investigate the application of the superposition theorem to multiple DC source circuits in terms of both voltage and current measurements. Power calculations will also be examined.

[4.1.1: Theory Overview](#)

[4.1.2: Equipment](#)

[4.1.3: Schematics](#)

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4.1.1: Theory Overview

The superposition theorem states that in a linear bilateral multi-source DC circuit, the current through or voltage across any particular element may be determined by considering the contribution of each source independently, with the remaining sources replaced with their internal resistance. The contributions are then summed, paying attention to polarities, to find the total value. Superposition cannot in general be applied to non-linear circuits or to non-linear functions such as power.

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4.1.2: Equipment

(1) Adjustable dual DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 4.7 k Ω

(1) 6.8 k Ω

(1) 10 k Ω

(1) 22 k Ω

(1) 33 k Ω

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4.1.3: Schematics

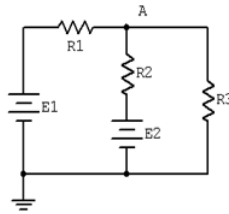


Figure 4.1.3.1

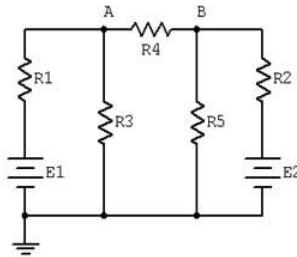


Figure 4.1.3.2

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4.1.4: Procedure

10.4.1: Voltage Application

1. Consider the dual supply circuit of Figure 10.3.1 using $E_1 = 10$ volts, $E_2 = 15$ volts, $R_1 = 4.7$ k, $R_2 = 6.8$ k and $R_3 = 10$ k. To find the voltage from node A to ground, superposition may be used. Each source is considered by itself. First consider source E_1 by assuming that E_2 is replaced with its internal resistance (a short). Determine the voltage at node A using standard series-parallel techniques and record it in Table 10.5.1. Make sure to indicate the polarity. Repeat the process using E_2 while shorting E_1 . Finally, sum these two voltages and record in Table 10.5.1.
2. To verify the superposition theorem, the process may be implemented directly by measuring the contributions. Build the circuit of Figure 10.3.1 with the values specified in step 1, however, replace E_2 with a short. Do not simply place a shorting wire across source E_2 ! This will overload the power supply.
3. Measure the voltage at node A and record in Table 10.5.1. Be sure to note the polarity.
4. Remove the shorting wire and insert source E_2 . Also, replace source E_1 with a short. Measure the voltage at node A and record in Table 10.5.1. Be sure to note the polarity.
5. Remove the shorting wire and re-insert source E_1 . Both sources should now be in the circuit. Measure the voltage at node A and record in Table 10.5.1. Be sure to note the polarity. Determine and record the deviations between theory and experimental results.

10.4.2: Current and Power Application

6. Consider the dual supply circuit of Figure 10.3.2 using $E_1 = 10$ volts, $E_2 = 15$ volts, $R_1 = 4.7$ k, $R_2 = 6.8$ k, $R_3 = 10$ k, $R_4 = 22$ k and $R_5 = 33$ k. To find the current through R_4 flowing from node A to B, superposition may be used. Each source is again treated independently with the remaining sources replaced with their internal resistances. Calculate the current through R_4 first considering E_1 and then considering E_2 . Sum these results and record the three values in Table 10.5.2.
7. Assemble the circuit of Figure 10.3.2 using the values specified. Replace source E_2 with a short and measure the current through R_4 . Be sure to note the direction of flow and record the result in Table 10.5.2.
8. Replace the short with source E_2 and swap source E_1 with a short. Measure the current through R_4 . Be sure to note the direction of flow and record the result in Table 10.5.2.
9. Remove the shorting wire and re-insert source E_1 . Both sources should now be in the circuit. Measure the current through R_4 and record in Table 10.5.2. Be sure to note the direction. Determine and record the deviations between theory and experimental results.
10. Power is not a linear function as it is proportional to the square of either voltage or current. Consequently, superposition should not yield an accurate result when applied directly to power. Based on the measured currents in Table 10.5.2, calculate the power in R_4 using E_1 -only and E_2 -only and record the values in Table 10.5.3. Adding these two powers yields the power as predicted by superposition. Determine this value and record it in Table 10.5.3. The true power in R_4 may be determined from the total measured current flowing through it. Using the experimental current measured when both E_1 and E_2 were active (Table 10.5.2), determine the power in R_4 and record it in Table 10.5.3.

10.4.3: Simulation

11. Build the circuit of Figure 10.3.2 in a simulator. Using the virtual DMM as an ammeter, determine the current through resistor R_4 and compare it to the theoretical and measured values recorded in Table 10.5.2.

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4.1.5: Data Tables

Source	V_A Theory	V_A Experimental	Deviation
E1 Only			
E2 Only			
E1 and E2			

Table 4.1.5.1

Source	I_{R4} Theory	I_{R4} Experimental	Deviation
E1 Only			
E2 Only			
E1 and E2			

Table 4.1.5.2

Source	P_{R4}
E1 Only	
E2 Only	
E1 + E2	
E1 and E2	

Table 4.1.5.3

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4.1.6: Questions

1. Based on the results of Tables 10.5.1, 10.5.2 and 10.5.3, can superposition be applied successfully to voltage, current and power levels in a DC circuit?
 2. If one of the sources in Figure 10.3.1 had been inserted with the opposite polarity, would there be a significant change in the resulting voltage at node A? Could both the magnitude and polarity change?
 3. If both of the sources in Figure 10.3.1 had been inserted with the opposite polarity, would there be a significant change in the resulting voltage at node A? Could both the magnitude and polarity change?
 4. Why is it important to note the polarities of the measured voltages and currents?
-

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SECTION OVERVIEW

4.2: Thévenin's Theorem

Objective

The objective of this exercise is to examine the use of Thévenin's Theorem to create simpler versions of DC circuits as an aide to analysis. Multiple methods of experimentally obtaining the Thévenin resistance will be explored.

[4.2.1: Theory Overview](#)

[4.2.2: Equipment](#)

[4.2.3: Schematics](#)

[4.2.4: Procedure](#)

[4.2.5: Data Tables](#)

[4.2.6: Questions](#)

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4.2.1: Theory Overview

Thévenin's Theorem for DC circuits states that any two port linear network may be replaced by a single voltage source with an appropriate internal resistance. The Thévenin equivalent will produce the same load current and voltage as the original circuit to any load. Consequently, if many different loads or subcircuits are under consideration, using a Thévenin equivalent may prove to be a quicker analysis route than “reinventing the wheel” each time.

The Thévenin voltage is found by determining the open circuit output voltage. The Thévenin resistance is found by replacing any DC sources with their internal resistances and determining the resulting combined resistance as seen from the two ports using standard series-parallel analysis techniques. In the laboratory, the Thévenin resistance may be found using an ohmmeter (again, replacing the sources with their internal resistances) or by using the matched load technique. The matched load technique involves replacing the load with a variable resistance and then adjusting it until the load voltage is precisely one half of the unloaded voltage. This would imply that the other half of the voltage must be dropped across the equivalent Thévenin resistance, and as the Thévenin circuit is a simple series loop then the two resistances must be equal as they have identical currents and voltages.

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4.2.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 2.2 k Ω

(1) 3.3 k Ω

(1) 4.7 k Ω

(1) 6.8 k Ω

(1) 8.2 k Ω

(1) 10 k potentiometer or resistance decade box

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4.2.3: Schematics

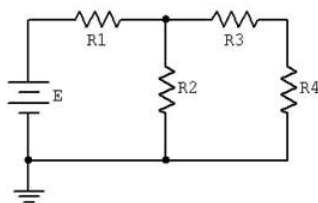


Figure 4.2.3.1

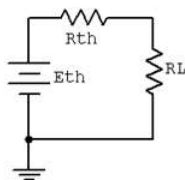


Figure 4.2.3.2

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4.2.4: Procedure

1. Consider the circuit of Figure 11.3.1 using $E = 10$ volts, $R_1 = 3.3$ k, $R_2 = 6.8$ k, $R_3 = 4.7$ k and $R_4 (R_{Load}) = 8.2$ k. This circuit may be analyzed using standard series-parallel techniques. Determine the voltage across the load, R_4 , and record it in Table 11.5.1. Repeat the process using 2.2 k for R_4 .
2. Build the circuit of Figure 11.3.1 using the values specified in step one, with $R_{Load} = 8.2$ k. Measure the load voltage and record it in Table 11.5.1. Repeat this with a 2.2 k load resistance. Determine and record the deviations. Do not deconstruct the circuit.
3. Determine the theoretical Thévenin voltage of the circuit of Figure 11.3.1 by finding the open circuit output voltage. That is, replace the load with an open and calculate the voltage produced between the two open terminals. Record this voltage in Table 11.5.2.
4. To calculate the theoretical Thévenin resistance, first remove the load and then replace the source with its internal resistance (ideally, a short). Finally, determine the combination series-parallel resistance as seen from the where the load used to be. Record this resistance in Table 11.5.2.
5. The experimental Thévenin voltage maybe determined by measuring the open circuit output voltage. Simply remove the load from the circuit of step one and then replace it with a voltmeter. Record this value in Table 11.5.2.
6. There are two methods to measure the experimental Thévenin resistance. For the first method, using the circuit of step one, replace the source with a short. Then replace the load with the ohmmeter. The Thévenin resistance may now be measured directly. Record this value in Table 11.5.2.
7. In powered circuits, ohmmeters are not effective while power is applied. An alternate method relies on measuring the effect of the load resistance. Return the voltage source to the circuit, replacing the short from step six. For the load, insert either the decade box or the potentiometer. Adjust this device until the load voltage is half of the open circuit voltage measured in step five and record in Table 11.5.2 under “Method 2”. At this point, the load and the Thévenin resistance form a simple series loop as seen in Figure 11.3.2. This means that they “see” the same current. If the load exhibits one half of the Thévenin voltage then the other half must be dropped across the Thévenin resistance, in other words $V_{RL} = V_{RTH}$. Consequently, the resistances have the same voltage and current, and therefore must have the same resistance according to Ohm’s law.
8. Consider the Thévenin equivalent of Figure 11.3.2 using the theoretical E_{TH} and R_{TH} from Table 11.5.2 along with 8.2 k for the load (R_L). Calculate the load voltage and record it in Table 11.5.3. Repeat the process for a 2.2 k load.
9. Build the circuit of Figure 11.3.2 using the measured E_{TH} and R_{TH} from Table 11.5.2 along with 8.2 k for the load (R_L). Measure the load voltage and record it in Table 11.5.3. Also determine and record the deviation.
10. Repeat step nine using a 2.2 k load.

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4.2.5: Data Tables

11.5.1: Original Circuit

R_4 (Load)	V_{Load} Theory	V_{Load} Experimental	Deviation
8.2 k			
2.2 k			

Table 4.2.5.1

11.5.2: Thévenized Circuit

	Theory	Experimental
E_{TH}		
R_{TH}		
R_{TH} Method 2	X	

Table 4.2.5.2

R_4 (Load)	V_{Load} Theory	V_{Load} Experimental	Deviation
8.2 k			
2.2 k			

Table 4.2.5.3

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4.2.6: Questions

1. Do the load voltages for the original and Thévenized circuits match for both loads? Is it logical that this could be extended to any arbitrary load resistance value?
2. Assuming several loads were under consideration, which is faster, analyzing each load with the original circuit of Figure 11.3.1 or analyzing each load with the Thévenin equivalent of Figure 11.3.2?
3. How would the Thévenin equivalent computations change if the original circuit contained more than one voltage source?

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SECTION OVERVIEW

4.3: Maximum Power Transfer

Objective

The objective of this exercise is to determine the conditions under which a load will produce maximum power. Further, the variance of load power and system efficiency will be examined graphically.

[4.3.1: Theory Overview](#)

[4.3.2: Equipment](#)

[4.3.3: Schematics](#)

[4.3.4: Procedure](#)

[4.3.5: Data Tables](#)

[4.3.6: Questions](#)

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4.3.1: Theory Overview

In order to achieve the maximum load power in a DC circuit, the load resistance must equal the driving resistance, that is, the internal resistance of the source. Any load resistance value above or below this will produce a smaller load power. System efficiency (η) is 50% at the maximum power case. This is because the load and the internal resistance form a basic series loop, and as they have the same value, they must exhibit equal currents and voltages, and hence equal powers. As the load increases in resistance beyond the maximizing value the load voltage will rise, however, the load current will drop by a greater amount yielding a lower load power. Although this is not the maximum load power, this will represent a larger percentage of total power produced, and thus a greater efficiency (the ratio of load power to total power).

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4.3.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) Resistance decade box

(1) 3.3 k Ω

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4.3.3: Schematics

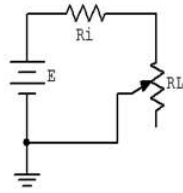


Figure 4.3.3.1

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4.3.4: Procedure

1. Consider the simple the series circuit of Figure 12.3.1 using $E = 10$ volts and $R_i = 3.3$ k. R_i forms a simple voltage divider with R_L . The power in the load is V_L^2 / R_L and the total circuit power is $E^2 / (R_i + R_L)$. The larger the value of R_L , the greater the load voltage, however, this does not mean that very large values of R_L will produce maximum load power due to the division by R_L . That is, at some point V_L^2 will grow more slowly than R_L itself. This crossover point should occur when R_L is equal to R_i . Further, note that as R_L increases, total circuit power decreases due to increasing total resistance. This should lead to an increase in efficiency. An alternate way of looking at the efficiency question is to note that as R_L increases, circuit current decreases. As power is directly proportional to the square of current, as R_L increases the power in R_i must decrease leaving a larger percentage of total power going to R_L .
2. Using $R_L = 30$, compute the expected values for load voltage, load power, total power and efficiency, and record them in Table 12.5.1. Repeat for the remaining R_L values in the Table. For the middle entry labeled Actual, insert the measured value of the 3.3 k used for R_i .
3. Build the circuit of Figure 12.3.1 using $E = 10$ volts and $R_i = 3.3$ k. Use the decade box for R_L and set it to 30 ohms. Measure the load voltage and record it in Table 12.5.2. Calculate the load power, total power and efficiency, and record these values in Table 12.5.2. Repeat for the remaining resistor values in the table.
4. Create two plots of the load power versus the load resistance value using the data from the two tables, one for theoretical, one for experimental. For best results make sure that the horizontal axis (R_L) uses a log scaling instead of linear.
5. Create two plots of the efficiency versus the load resistance value using the data from the two tables, one for theoretical, one for experimental. For best results make sure that the horizontal axis (R_L) uses a log scaling instead of linear.

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4.3.5: Data Tables

R_L	V_L	P_L	P_T	η
30				
150				
500				
1 k				
2.5 k				
Actual=				
4 k				
10 k				
25 k				
70 k				
300 k				

Table 4.3.5.1

R_L	V_L	P_L	P_T	η
30				
150				
500				
1 k				
2.5 k				
Actual=				
4 k				
10 k				
25 k				
70 k				
300 k				

Table 4.3.5.2

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4.3.6: Questions

1. At what point does maximum load power occur?
 2. At what point does maximum total power occur?
 3. At what point does maximum efficiency occur?
 4. Is it safe to assume that generation of maximum load power is always a desired goal? Why/why not?
-

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CHAPTER OVERVIEW

5: Circuit Analysis Techniques

5.1: Nodal Analysis

5.1.1: Theory Overview

5.1.2: Equipment

5.1.3: Schematics

5.1.4: Procedure

5.1.5: Data Tables

5.1.6: Questions

5.2: Mesh Analysis

5.2.1: Theory Overview

5.2.2: Equipment

5.2.3: Schematics

5.2.4: Procedure

5.2.5: Data Tables

5.2.6: Questions

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SECTION OVERVIEW

5.1: Nodal Analysis

Objective

The study of nodal analysis is the objective of this exercise, specifically its usage in multi-source DC circuits. Its application to finding circuit currents and voltages will be investigated.

[5.1.1: Theory Overview](#)

[5.1.2: Equipment](#)

[5.1.3: Schematics](#)

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[5.1.5: Data Tables](#)

[5.1.6: Questions](#)

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5.1.1: Theory Overview

Multi-source DC circuits may be analyzed using a node voltage technique. The process involves identifying all of the circuit nodes, a node being a point where various branch currents combine. A reference node, usually ground, is included. Kirchhoff's current law is then applied to each node. Consequently a set of simultaneous equations are created with an unknown voltage for each node with the exception of the reference. In other words, a circuit with a total of five nodes including the reference will yield four unknown node voltages and four equations. Once the node voltages are determined, various branch currents and component voltages may be derived.

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5.1.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 4.7 k Ω

(1) 6.8 k Ω

(1) 10 k Ω

(1) 22 k Ω

(1) 33 k Ω

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5.1.3: Schematics

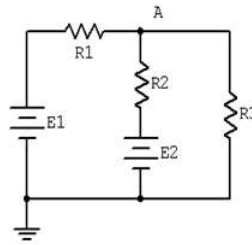


Figure 5.1.3.1

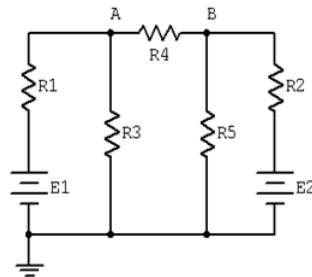


Figure 5.1.3.2

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5.1.4: Procedure

1. Consider the dual supply circuit of Figure 13.3.1 using $E_1 = 10$ volts, $E_2 = 15$ volts, $R_1 = 4.7$ k, $R_2 = 6.8$ k and $R_3 = 10$ k. To find the voltage from node A to ground, nodal analysis may be applied. In this circuit note that there is only one node and therefore only one equation with one unknown is needed. Once this potential is found, all other circuit currents and voltages may be found by applying Ohm's law and/or KVL and KCL.
2. Write the node equation for the circuit of Figure 13.3.1 and solve for node voltage A. Also, determine the current through R_3 . Record these values in Table 13.5.1.
3. Construct the circuit of Figure 13.3.1 using the values specified in step one. Measure the voltage from node A to ground along with the current through R_3 . Record these values in Table 13.5.1. Also determine and record the deviations.
4. Consider the dual supply circuit of Figure 13.3.2 using $E_1 = 10$ volts, $E_2 = 15$ volts, $R_1 = 4.7$ k, $R_2 = 6.8$ k, $R_3 = 10$ k, $R_4 = 22$ k and $R_5 = 33$ k. Applying nodal analysis to this circuit yields two equations with two unknowns, namely node voltages A and B. Again, once these potentials are found, any other circuit current or voltage may be determined by applying Ohm's law and/or KVL and KCL.
5. Write the node equations for the circuit of Figure 13.3.2 and solve for node voltage A, node voltage B and the potential from A to B. Also, determine the current through R_4 . Record these values in Table 13.5.2.
6. Construct the circuit of Figure 13.3.2 using the values specified in step four. Measure the voltages from node A to ground, node B to ground and from node A to B, along with the current through R_4 . Record these values in Table 13.5.2. Also determine and record the deviations.

13.4.1: Simulation

7. Build the circuit of Figure 13.3.2 in a simulator. Using the DC Operating Point simulation function, determine the voltages at nodes A and B, and compare these to the theoretical and measured values recorded in Table 13.5.2.

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5.1.5: Data Tables

Parameter	Theory	Experimental	Deviation
V_A			
I_{R3}			

Table 5.1.5.1

Parameter	Theory	Experimental	Deviation
V_A			
V_B			
V_{AB}			
I_{R4}			

Table 5.1.5.2

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5.1.6: Questions

1. Do the polarities of the sources in Figure 13.3.1 matter as to the resulting voltages? Will the magnitudes of the voltages be the same if one or both sources have an inverted polarity?
 2. In both circuits of this exercise the negative terminals of the sources are connected to ground. Is this a requirement for nodal analysis? What would happen to the node voltages if the positions of E1 and R1 in Figure 13.3.1 were swapped?
 3. The circuits of Figures 13.3.1 and 13.3.2 had been analyzed previously in the Superposition Theorem exercise. How do the results of this exercise compare to the earlier results? Should the resulting currents and voltages be identical? If not, what sort of things might affect the outcome?
-

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SECTION OVERVIEW

5.2: Mesh Analysis

Objective

The study of mesh analysis is the objective of this exercise, specifically its usage in multi-source DC circuits. Its application to finding circuit currents and voltages will be investigated.

[5.2.1: Theory Overview](#)

[5.2.2: Equipment](#)

[5.2.3: Schematics](#)

[5.2.4: Procedure](#)

[5.2.5: Data Tables](#)

[5.2.6: Questions](#)

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5.2.1: Theory Overview

Multi-source DC circuits may be analyzed using a mesh current technique. The process involves identifying a minimum number of small loops such that every component exists in at least one loop. Kirchhoff's voltage law is then applied to each loop. The loop currents are referred to as mesh currents as each current interlocks or meshes with the surrounding loop currents. As a result there will be a set of simultaneous equations created, an unknown mesh current for each loop. Once the mesh currents are determined, various branch currents and component voltages may be derived.

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5.2.2: Equipment

(1) Adjustable DC power supply

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) 4.7 k Ω

(1) 6.8 k Ω

(1) 10 k Ω

(1) 22 k Ω

(1) 33 k Ω

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5.2.3: Schematics

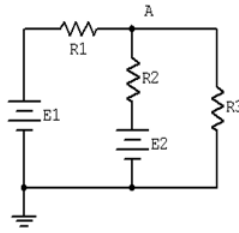


Figure 5.2.3.1

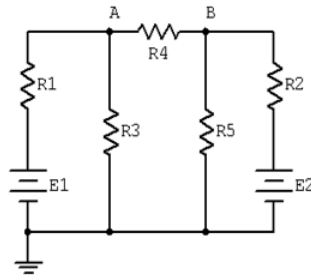


Figure 5.2.3.2

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5.2.4: Procedure

1. Consider the dual supply circuit of Figure 14.3.1 using $E_1 = 10$ volts, $E_2 = 15$ volts, $R_1 = 4.7$ k, $R_2 = 6.8$ k and $R_3 = 10$ k. To find the voltage from node A to ground, mesh analysis may be used. This circuit may be described via two mesh currents, loop one formed with E_1 , R_1 , R_2 and E_2 , and loop two formed with E_2 , R_2 and R_3 . Note that these mesh currents are the currents flowing through R_1 and R_3 respectively.
2. Using KVL, write the loop expressions for these two loops and then solve to find the mesh currents. Note that the third branch current (that of R_2) is the combination of the mesh currents and that the voltage at node A can be determined using the second mesh current and Ohm's law. Compute these values and record them in Table 14.5.1.
3. Build the circuit of Figure 14.3.1 using the values specified in step one. Measure the three branch currents and the voltage at node A and record in Table 14.5.1. Be sure to note the directions and polarities. Finally, determine and record the deviations in Table 14.5.1.
4. Consider the dual supply circuit of Figure 14.3.2 using $E_1 = 10$ volts, $E_2 = 15$ volts, $R_1 = 4.7$ k, $R_2 = 6.8$ k, $R_3 = 10$ k, $R_4 = 22$ k and $R_5 = 33$ k. This circuit will require three loops to describe fully. This means that there will be three mesh currents in spite of the fact that there are five branch currents. The three mesh currents correspond to the currents through R_1 , R_2 , and R_4 .
5. Using KVL, write the loop expressions for these loops and then solve to find the mesh currents. Note that the voltages at nodes A and B can be determined using the mesh currents and Ohm's law. Compute these values and record them in Table 14.5.2.
6. Build the circuit of Figure 14.3.2 using the values specified in step four. Measure the three mesh currents and the voltages at node A, node B, and from node A to B, and record in Table 14.5.2. Be sure to note the directions and polarities. Finally, determine and record the deviations in Table 14.5.2.

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5.2.5: Data Tables

Parameter	Theory	Experimental	Deviation
I_{R1}			
I_{R2}			
I_{R3}			
V_A			

Table 5.2.5.1

Parameter	Theory	Experimental	Deviation
I_{R1}			
I_{R2}			
I_{R4}			
V_A			
V_B			
V_{AB}			

Table 5.2.5.2

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5.2.6: Questions

1. Do the polarities of the sources in Figure 14.3.1 matter as to the resulting currents? Will the magnitudes of the currents be the same if one or both sources have an inverted polarity?
 2. In both circuits of this exercise the negative terminals of the sources are connected to ground. Is this a requirement for mesh analysis? What would happen to the mesh currents if the positions of E1 and R1 in Figure 14.3.1 were swapped?
 3. The circuits of Figures 14.3.1 and 14.3.2 had been analyzed previously in the Superposition Theorem and Nodal Analysis exercises. How do the results of this exercise compare to the earlier results? Should the resulting currents and voltages be identical? If not, what sort of things might affect the outcome?
 4. In general, compare and contrast the application of Superposition, Mesh and Nodal Analyses to multisource DC circuits. What are the advantages and disadvantages of each? Are some circuits better approached with a particular technique? Will each technique enable any particular current or voltage to be found or are there limitations?
-

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CHAPTER OVERVIEW

6: First Order Circuits

6.1: Capacitors

6.1.1: Introduction

6.1.2: Capacitance and Capacitors

6.1.3: Initial and Steady-State Analysis of RC Circuits

6.1.4: Transient Response of RC Circuits

6.1.5: Summary

6.1.6: Exercises

6.2: Inductors

6.2.1: Introduction

6.2.2: Inductance and Inductors

6.2.3: Initial and Steady-State Analysis of RL Circuits

6.2.4: Initial and Steady-State Analysis of RLC Circuits

6.2.5: Transient Response of RL Circuits

6.2.6: Summary

6.2.7: Exercises

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SECTION OVERVIEW

6.1: Capacitors

Learning Objectives

After completing this chapter, you should be able to:

- Describe the theoretical and practical aspects of capacitor construction.
- Describe the current-voltage characteristic behavior of capacitors.
- Utilize component data sheets to determine operating characteristics of capacitors.
- Determine the initial and steady-state equivalents of resistor-capacitor networks.
- Determine the transient response of basic RC networks.

[6.1.1: Introduction](#)

[6.1.2: Capacitance and Capacitors](#)

[6.1.3: Initial and Steady-State Analysis of RC Circuits](#)

[6.1.4: Transient Response of RC Circuits](#)

[6.1.5: Summary](#)

[6.1.6: Exercises](#)

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6.1.1: Introduction

This chapter introduces another passive device, the capacitor. Capacitors are fundamentally different from resistors in terms of both their construction and their operation. For starters, when placed in DC circuits, capacitors are not ohmic, unlike resistors. Their current-voltage characteristic does not respond to Ohm's law. Instead, their current-voltage characteristic is dynamic in nature. Further, in the ideal case, capacitors do not dissipate power. Indeed, capacitors are energy storage devices. In a way, you could imagine them to be a little like rechargeable batteries, but unlike batteries these devices could be charged or discharged in tiny fractions of a second and last for billions upon billions of cycles.

Capacitors are an integral part of modern electronic systems. They are used in AC-to-DC power supplies to help smooth and stabilize the output voltage. In audio and communications systems they are used in filters, for example to control the high and low frequency response of amplifiers and similar equipment, or for tuning purposes. Essentially, in any application that needs to smooth out a varying voltage, store electric charge or filter a signal; a capacitor is likely to be used.

Much of the original work on capacitors was done in the 18th century. One of the earliest examples of a capacitor was the Leyden jar, which consists of a glass bottle or jar lined with metal foil on the inside and the outside. Benjamin Franklin's famous kite experiment made use of a Leyden jar. In the early days, capacitors were known as condensers (not to be confused with the condensers used in air conditioning systems).

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6.1.2: Capacitance and Capacitors

A capacitor is a device that stores energy. Capacitors store energy in the form of an electric field. At its most simple, a capacitor can be little more than a pair of metal plates separated by air. As this constitutes an open circuit, DC current will not flow through a capacitor. If this simple device is connected to a DC voltage source, as shown in Figure 8.2.1, negative charge will build up on the bottom plate while positive charge builds up on the top plate. This process will continue until the voltage across the capacitor is equal to that of the voltage source. In the process, a certain amount of electric charge will have accumulated on the plates.

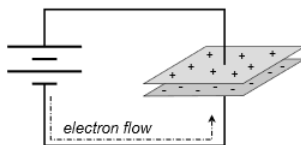


Figure 8.2.1 : Basic capacitor with voltage source.

The ability of this device to store charge with regard to the voltage appearing across it is called capacitance. Its symbol is C and it has units of farads (F), in honor of Michael Faraday, a 19th century English scientist who did early work in electromagnetism. By definition, if a total charge of 1 coulomb is associated with a potential of 1 volt across the plates, then the capacitance is 1 farad.

$$1 \text{ farad} \equiv 1 \text{ coulomb} / 1 \text{ volt} \quad (6.1.2.1)$$

or more generally,

$$C = \frac{Q}{V} \quad (6.1.2.2)$$

Where

C is the capacitance in farads,

Q is the charge in coulombs,

V is the voltage in volts.

From Equation 6.1.2.2 we can see that, for any given voltage, the greater the capacitance, the greater the amount of charge that can be stored. We can also see that, given a certain size capacitor, the greater the voltage, the greater the charge that is stored. These observations relate directly to the amount of energy that can be stored in a capacitor.

Unsurprisingly, the energy stored in capacitor is proportional to the capacitance. It is also proportional to the square of the voltage across the capacitor.

$$W = \frac{1}{2} CV^2 \quad (6.1.2.3)$$

Where

W is the energy in joules,

C is the capacitance in farads,

V is the voltage in volts.

The basic capacitor consists of two conducting plates separated by an insulator, or dielectric. This material can be air or made from a variety of different materials such as plastics and ceramics. This is depicted in Figure 8.2.2.

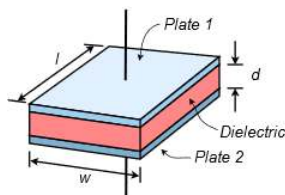


Figure 8.2.2 : Components of a generic capacitor.

For practical capacitors, the plates may be stacked alternately or even made of foil and formed into a rolled tube. However it is constructed, the characteristics of the dielectric will play a major role in the performance of the device, as we shall see.

In general, capacitance increases directly with plate area, A , and inversely with plate separation distance, d . Further, it is also proportional to a physical characteristic of the dielectric; the permittivity, ϵ . Thus, capacitance is equal to:

$$C = \epsilon \frac{A}{d} \quad (6.1.2.4)$$

Where

C is the capacitance in farads,

A is the plate area in square meters,

d is the plate separation distance in meters,

ϵ is permittivity of the dielectric between the plates.

It should be noted that the effective plate area is somewhat larger than the precise physical area of the plates. This is due to a phenomenon called fringing. Essentially, the electric field lines bulge outward at the plate edges rather than maintain uniform parallel orientation. This is illustrated in Figure 8.2.3

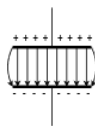


Figure 8.2.3 : Capacitor electric field with fringing.

From Equation 6.1.2.4 it is obvious that the permittivity of the dielectric plays a major role in determining the volumetric efficiency of the capacitor, in other words, the amount of capacitance that can be packed into a given sized component. Some dielectrics are notably more efficient than others. To make comparisons easier, relative permittivity is often used, that is, the ratio of the dielectric's permittivity to that of a vacuum, ϵ_0 .

A table of relative permittivity for a variety of dielectrics is shown in Table 8.2.1 . A number of common dielectrics, such as various poly plastic films and mica, exhibit permittivities two to six times that of air, but there are also ceramic dielectrics whose dielectrics are hundreds to thousands of times that of air.

Table 8.2.1 : Relative permittivity of various dielectrics. Data derived from Wikipedia and other sources.

Material	Relative permittivity, $\epsilon_r = \epsilon/\epsilon_0$
Vacuum	1 ($\epsilon_0 = 8.85\text{E-}12$ farads/meter)
Air	1.00058986 (at STP)
PTFE/Teflon	2.1
Polyethylene/XLPE	2.25
Polyimide	3.4
Polypropylene	2.2-2.36
Polystyrene	2.4-2.7
Polyester (Mylar)	3.1
Paper	1.4
Mica	3-6
Silicon dioxide	3.9
Rubber	7
Diamond	5.5-10
Silicon	11.68
Titanium dioxide	86-173
Strontium titanate	310
Calcium copper titanate	>250,000

At quick glance, it might seem that choosing the dielectric with the highest permittivity would be the best choice but this is not necessarily the case. There are several other factors that go into this decision including temperature stability, leakage resistance (effective parallel resistance), ESR (equivalent series resistance) and breakdown strength. For an ideal capacitor, leakage resistance would be infinite and ESR would be zero.

Unlike resistors, capacitors do not have maximum power dissipation ratings. Instead, they have maximum voltage ratings. The breakdown strength of the dielectric will set an upper limit on how large of a voltage may be placed across a capacitor before it is damaged. Breakdown strength is measured in volts per unit distance, thus, the closer the plates, the less voltage the capacitor can withstand. For example, halving the plate distance doubles the capacitance but also halves its voltage rating. Table 8.2.2 lists the breakdown strengths of a variety of different dielectrics. Comparing the tables of Tables 8.2.1 and 8.2.2 hints at the complexity of the situation. For instance, consider polystyrene versus polypropylene. Polystyrene offers modestly increased permittivity yet polypropylene has a considerable advantage in terms of breakdown strength. As a consequence, the plates can be placed much closer together when using polypropylene while achieving the same voltage rating as a capacitor using polystyrene. Therefore, the polypropylene capacitor will require less volume for the same capacitance. As an added benefit, polypropylene exhibits high temperature stability and low moisture absorption, among other characteristics. Comparing polypropylene to polyester, we find that polyester's improved permittivity along with a similar breakdown strength yields improved volumetric efficiency over polypropylene. Unfortunately, polyester suffers from greater temperature dependence.

Table 8.2.2 : Dielectric strength of various dielectrics. Data derived from Wikipedia and other sources.c

Substance	Breakdown Strength (kV/mm)
Air	3.0
Borosilicate glass	20-40
PTFE (Teflon, insulating film)	60-173
Polyethylene	19-160
Polypropylene	650
Polystyrene	19.7
PEEK (Polyether ether ketone)	23
Polyester (Mylar)	580
Neoprene rubber	15.7-26.7
Distilled water	65-70
Waxed paper	40-60
Mica	118
Diamond	2,000
PZT (ceramic)	10-25

Capacitor Styles and Packaging

Capacitors are available in a wide range of capacitance values, from just a few picofarads to well in excess of a farad, a range of over 10^{12} . Unlike resistors, whose physical size relates to their power rating and not their resistance value, the physical size of a capacitor is related to both its capacitance and its voltage rating (a consequence of Equation 6.1.2.4. Modest surface mount capacitors can be quite small while the power supply filter capacitors commonly used in consumer electronics devices such as an audio amplifier can be considerably larger than a D cell battery. A sampling of capacitors is shown in Figure 8.2.4 .



Figure 8.2.4 : A variety of capacitor styles and packages.

Toward the front and left side of the photo are a variety of plastic film capacitors. The disk-shaped capacitor uses a ceramic dielectric. The small square device toward the front is a surface mount capacitor, and to its right is a teardrop-shaped tantalum capacitor, commonly used for power supply bypass applications in electronic circuits. The medium sized capacitor to the right with folded leads is a paper capacitor, at one time very popular in audio circuitry. A number of capacitors have a crimp ring at one side, including the large device with screw terminals. These are aluminum electrolytic capacitors. These devices tend to exhibit high volumetric efficiency but generally do not offer top performance in other areas such as absolute accuracy and leakage current. They usually are polarized, meaning that the leads must match the polarity of the applied voltage. Inserting them into a circuit backwards can result in catastrophic failure. The polarity is usually identified by a series of minus signs and/or a stripe that indicates the

negative lead. Tantalum capacitors are also polarized but are typically denoted with a plus sign next to the positive lead. A variable capacitor used for tuning radios is shown in Figure 8.2.5 . One set of plates is fixed to the frame while an intersecting set of plates is affixed to a shaft. Rotating the shaft changes the amount of plate area that overlaps, and thus changes the capacitance.



Figure 8.2.5 : A variable capacitor.

For large capacitors, the capacitance value and voltage rating are usually printed directly on the case. Some capacitors use “MFD” which stands for “microfarads”. While a capacitor color code exists, rather like the resistor color code, it has generally fallen out of favor. For smaller capacitors a numeric code is used that echoes the color code. Typically it consists of a three digit number such as “152”.

The first two digits are the precision portion and the third digit is the power of ten multiplier. The result is in picofarads. Thus, 152 is 1500 pf.

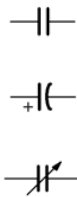


Figure 8.2.6 : Capacitor schematic symbols (top-bottom): non-polarized, polarized, variable.

The schematic symbols for capacitors are shown in Figure 8.2.6 . There are three symbols in wide use. The first symbol, using two parallel lines to echo the two plates, is for standard non-polarized capacitors. The second symbol represents polarized capacitors. In this variant, the positive lead is drawn with a straight line for that plate and often denoted with a plus sign. The negative terminal is drawn with a curved line. The third symbol is used for variable capacitors and is drawn with an arrow through it, rather like a rheostat.



Figure 8.2.7 : An LCR meter, designed to read capacitance, resistance and inductance.

In order to obtain accurate measurements of capacitors, an LCR meter, such as the one shown in Figure 8.2.7 , may be used. These devices are designed to measure the three common passive electrical components: resistors, capacitors and inductors¹. Unlike a simple digital multimeter, an LCR meter can also measure the values at various AC frequencies instead of just DC, and also determine secondary characteristics such as equivalent series resistance and effective parallel leakage resistance.

Capacitor Data Sheet

A portion of a typical capacitor data sheet is shown in Figure 8.2.8 . This is for a series of through-hole style metallized film capacitors using polypropylene for the dielectric. First we see a listing of general features. For starters, we find that the capacitors use a flame retardant epoxy coating and are also RoHS compliant. We then move to a set of electrical performance specifications. For example, we see that this series is available in two variants, one rated at 800 volts DC and the other rated at 1600 volts DC. Further, tolerance is available as either $\pm 3\%$ or $\pm 5\%$. Dissipation factor ($\tan \delta$) is a measure of particular importance for AC

Find the equivalent capacitance of the network shown in Figure 8.2.10 .

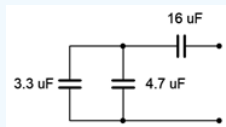


Figure 8.2.10 : Circuit for Example 8.2.2 .

In this circuit, we find that the left and middle capacitors are in parallel. This combination is in series with the capacitor to the right:

$$C_{left} = C_1 + C_2$$

$$C_{left} = 3.3\mu F + 4.7\mu F$$

$$C_{left} = 8\mu F$$

$$C_{Total} = \frac{C_{left}C_3}{C_{left} + C_3}$$

$$C_{Total} = \frac{8\mu F 16\mu F}{8\mu F + 16\mu F}$$

$$C_{Total} \approx 5.33\mu F$$

If a circuit contains nothing but a voltage source in parallel with a group of capacitors, the voltage will be the same across all of the capacitors, just as it is in a resistive parallel circuit. If the circuit instead consists of multiple capacitors that are in series with a voltage source, as shown in Figure 8.2.11 , the voltage will divide between them in inverse proportion. In other words, the larger the capacitance, the smaller its share of the applied voltage. The voltages can also be found by first determining the series equivalent capacitance. The total charge may then be determined using the applied voltage. Finally, the individual voltages are computed from Equation 6.1.2.2, $V = Q/C$, where Q is the total charge and C is the capacitance of interest. This is illustrated in the following example.

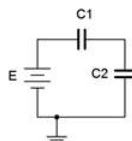


Figure 8.2.11 : A simple capacitors-only series circuit.

✓ Example 8.2.3

Find the voltages across the capacitors in Figure 8.2.12 .

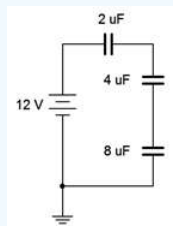


Figure 8.2.12 : Circuit for Example 8.2.3 .

The first step is to determine the total capacitance. As these are in series, we can use the reciprocal rule:

$$C_{Total} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}$$

$$C_{Total} = \frac{1}{\frac{1}{2\mu F} + \frac{1}{4\mu F} + \frac{1}{8\mu F}}$$

$$C_{Total} \approx 1.143\mu F$$

From here we determine the total charge:

$$Q = VC$$

$$Q = 12V1.143\mu F$$

$$Q = 13.71\mu C$$

Charge is constant across all of the series capacitors, therefore:

$$V_{2\mu F} = \frac{Q}{C}$$

$$V_{2\mu F} = \frac{13.71\mu C}{2\mu F}$$

$$V_{2\mu F} = 6.855V$$

$$V_{4\mu F} = \frac{Q}{C}$$

$$V_{4\mu F} = \frac{13.71\mu C}{4\mu F}$$

$$V_{4\mu F} = 3.427V$$

$$V_{8\mu F} = \frac{Q}{C}$$

$$V_{8\mu F} = \frac{13.71\mu C}{8\mu F}$$

$$V_{8\mu F} = 1.714V$$

The sum of the three voltages is 12 volts (within rounding error) and verifies KVL as expected.

Practical Tip

While it may be tempting to try, do not attempt to verify the operation of Example 8.2.3 in the laboratory using a standard DMM. The reason is because the internal resistance of a typical digital voltmeter is many orders of magnitude lower than the leakage resistance of the capacitors. As a result, charge will be transferred to the meter, ruining the measurement. It would be akin to trying to measure the voltages across a string of resistors, each in excess of 100 MΩ, with a meter whose internal resistance is 1 MΩ. The meter's resistance dominates the parallel combination and causes excessive loading which ruins the measurement. A special sort of voltmeter, an electrostatic voltmeter or electrometer, is needed for these types of measurements. These are sometimes referred to as non-charge transfer meters.

Current-Voltage Relationship

The fundamental current-voltage relationship of a capacitor is not the same as that of resistors. Capacitors do not so much resist current; it is more productive to think in terms of them reacting to it. The current through a capacitor is equal to the capacitance times the rate of change of the capacitor voltage with respect to time (i.e., its slope). That is, the value of the voltage is not important, but rather how quickly the voltage is changing. Given a fixed voltage, the capacitor current is zero and thus the capacitor behaves like an open. If the voltage is changing rapidly, the current will be high and the capacitor behaves more like a short. Expressed as a formula:

$$i = C \frac{dv}{dt} \quad (6.1.2.5)$$

Where

i is the current flowing through the capacitor,

C is the capacitance,

dv/dt is the rate of change of capacitor voltage with respect to time.

A particularly useful form of Equation 6.1.2.5 is:

$$\frac{dv}{dt} = \frac{i}{C} \quad (6.1.2.6)$$

An alternate way of looking at Equation 6.1.2.5 indicates that if a capacitor is fed by a constant current source, the voltage will rise at a constant rate (dv/dt). It is continuously depositing charge on the plates of the capacitor at a rate of I , which is equivalent to Q/t . As long as the current is present, feeding the capacitor, the voltage across the capacitor will continue to rise. A good analogy is if we had a pipe pouring water into a tank, with the tank's level continuing to rise. This process of depositing charge on the plates is referred to as charging the capacitor. For example, considering the circuit in Figure 8.2.13, we see a current source feeding a single capacitor. If we were to plot the capacitor's voltage over time, we would see something like the graph of Figure 8.2.14.

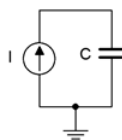


Figure 8.2.13 : Capacitor with current source.

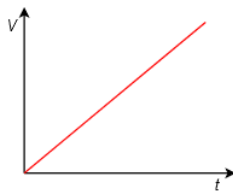


Figure 8.2.14 : Capacitor voltage versus time.

As time progresses, the voltage across the capacitor increases with a positive polarity from top to bottom. With a theoretically perfect capacitor and source, this would continue forever, or until the current source was turned off. In reality, this line would either begin to deflect horizontally as the source reached its limits, or the capacitor would fail once its breakdown voltage was reached. The slope of this line is dictated by the size of the current source and the capacitance.

✓ Example 8.2.4

Determine the rate of change of voltage across the capacitor in the circuit of Figure 8.2.15. Also determine the capacitor's voltage 10 milliseconds after power is switched on.

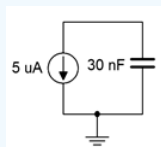


Figure 8.2.15 : Circuit for Example 8.2.4.

First, note the direction of the current source. This will produce a negative voltage across the capacitor from top to bottom. The rate of change is:

$$\frac{dv}{dt} = \frac{i}{C}$$

$$\frac{dv}{dt} = \frac{-5\mu A}{30nF}$$

$$\frac{dv}{dt} \approx -166.7 \text{ volts per second}$$

Thus, for every second, the voltage rises another -166.7 volts. Assuming it is completely uncharged when power is applied, after 10 milliseconds it will have risen to -166.7 V/s times 10 ms, or -1.667 volts.

Equation 6.1.2.6 provides considerable insight into the behavior of capacitors. As just noted, if a capacitor is driven by a fixed current source, the voltage across it rises at the constant rate of i/C . There is a limit to how quickly the voltage across the capacitor can change. An instantaneous change means that dv/dt is infinite, and thus, the current driving the capacitor would also have to be infinite (an impossibility). This is not an issue with resistors, which obey Ohm's law, but it is a limitation of capacitors. Therefore we can state a particularly important characteristic of capacitors:

The voltage across a capacitor cannot change instantaneously. (6.1.2.7)

This observation will be key to understanding the operation of capacitors in DC circuits.

References

¹Inductors are the subject of the next chapter.

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6.1.3: Initial and Steady-State Analysis of RC Circuits

When analyzing resistor-capacitor circuits, always remember that capacitor voltage cannot change instantaneously. If we assume that a capacitor in a circuit is not initially charged, then its voltage must be zero. The instant the circuit is energized, the capacitor voltage must still be zero. If there is no voltage across the device, then it is behaving like a short circuit. We call this the initial state. Thus, we have our first rule regarding RC circuits:

For DC analysis, initially capacitors appear as shorts. (6.1.3.1)

Consider the circuit of Figure 8.3.1. Assume that C_1 and C_2 are initially uncharged and there is no voltage across them.

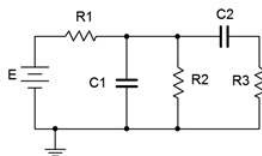


Figure 8.3.1 : A basic resistor-capacitor (RC) circuit.

The instant power is applied, the two capacitors appear as short circuits. If we redraw the circuit for this instant in time, we arrive at the equivalent circuit shown in Figure 8.3.2.

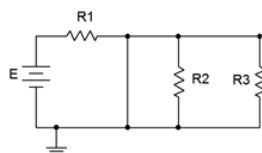


Figure 8.3.2 : A basic RC circuit, initial state.

Given this equivalent, we can see that shorting C_2 places R_2 and R_3 in parallel, however, they are both shorted out by C_1 . This leaves only R_1 left in the circuit along with the source, E . At this point, currents will begin to flow, and thus begin charging up the capacitors. As the capacitor voltages rise, the current will begin to decrease, and eventually the capacitors will stop charging. At that point no further current will be flowing, and thus the capacitor will behave like an open. We call this the steady-state condition and we can state our second rule:

At steady-state, capacitors appear as opens. (6.1.3.2)

Continuing with the example, at steady-state both capacitors behave as opens. This is shown in Figure 8.3.3. This leaves E to drop across R_1 and R_2 . This will create a simple voltage divider. The steady-state voltage across C_1 will equal that of R_2 . As C_2 is also open, the voltage across R_3 will be zero while the voltage across C_2 will be the same as that across R_2 .

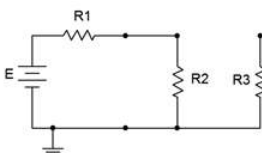


Figure 8.3.3 : A basic RC circuit, steady-state.

In reality, practical capacitors can be thought of as an ideal capacitance in parallel with a very large (leakage) resistance, so there will be a limit to this performance.

✓ Example 8.3.1

Given the circuit of Figure 8.3.4, find the voltage across the $6\text{ k}\Omega$ resistor for both the initial and steady-state conditions assuming the capacitor is initially uncharged.

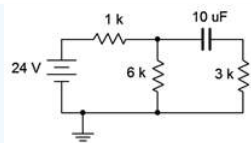


Figure 8.3.4 : Circuit for Example 8.2.4.

For the initial state the capacitor is treated as a short. The initial state equivalent circuit is drawn below in Figure 8.3.5 . Immediately apparent is the parallel connection between the 6 kΩ and 3 kΩ resistors. This combination is equivalent to 2 kΩ. Therefore, we can perform a voltage divider to find the potential across the 6 kΩ (i.e., the 2 kΩ combo).

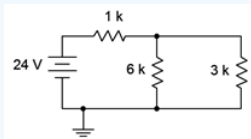


Figure 8.3.5 : Circuit of Figure 8.3.3 , initial state.

$$V_{6k} = E \frac{R_x}{R_x + R_y}$$

$$V_{6k} = 24V \frac{2k\Omega}{2k\Omega + 1k\Omega}$$

$$V_{6k} = 16V$$

For the steady-state condition the capacitor will be fully charged, its current will be zero, and we treat it as an open. The steady-state equivalent circuit is drawn below in Figure 8.3.6 .

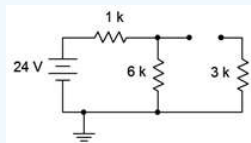


Figure 8.3.6 : Circuit of Figure 8.3.3 , steady-state.

The 3 kΩ resistor is now out of the picture, leaving us with the 6 kΩ in series with the 1 kΩ resistor. Once again, a voltage divider may be used to determine the voltage across the 6 kΩ.

$$V_{6k} = E \frac{R_x}{R_x + R_y}$$

$$V_{6k} = 24V \frac{6k\Omega}{6k\Omega + 1k\Omega}$$

$$V_{6k} = 20.57V$$

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6.1.4: Transient Response of RC Circuits

The question remains, “What happens between the time the circuit is powered up and when it reaches steady-state?” This is known as the transient response. Consider the circuit shown in Figure 8.4.1 . Note the use of a voltage source rather than a fixed current source, as examined earlier.

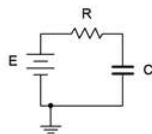


Figure 8.4.1 : A simple RC circuit.

The key to the analysis is to remember that capacitor voltage cannot change instantaneously. Assuming the capacitor is uncharged, the instant power is applied, the capacitor voltage must be zero. Therefore all of the source voltage drops across the resistor. This creates the initial current, and this current starts to charge the capacitor (the initial rate being equal to i/C as dictated by Equation 8.2.6). According to Kirchhoff's voltage law, as the capacitor voltage begins to increase, the resistor voltage must decrease because the sum of the two must equal the fixed source voltage. This means that the circulating current must also decrease. This, in turn, means that the rate of capacitor voltage increase begins to slow. As the capacitor voltage continues to increase, less voltage is available for the resistor, causing further reductions in current, and a further slowing of the rate of capacitor voltage change. Eventually, the capacitor voltage will be nearly equal to the source voltage. This will result in a very small potential across the resistor and an equally small current, slowing subsequent capacitor voltage increases to a near standstill. Theoretically, the capacitor voltage approaches the source voltage but never quite equals it. Similarly, the current drops to near zero, but never completely turns off. This is illustrated in Figure 8.4.2 .

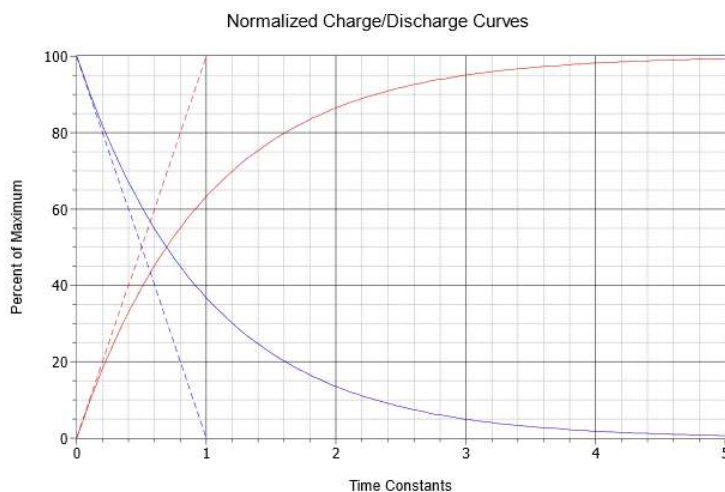


Figure 8.4.2 : Normalized charge and discharge curves.

The dashed red line represents the initial rate of change of capacitor voltage. This trajectory is what would be expected if an ideal current source drove the capacitor, as in Example 8.2.4. As noted previously, the rate of voltage change versus times is equal to i/C , and therefore in this case, E/RC . If the initial rate of change were to continue unabated, the source voltage, E , would be reached in RC seconds. Consequently, RC is referred to as the charge time constant and is denoted by τ (Greek letter tau). Thus,

$$\text{Time constant, } \tau = RC \quad (6.1.4.1)$$

As noted, once the capacitor begins to charge, the current begins to decrease and the capacitor voltage curve begins to fall away from the initial trajectory. The solid red curve represents the capacitor voltage. Notice that after five time constants the capacitor is nearly fully charged and the circuit is considered to be in steady-state (i.e., the capacitor behaves as an open).

$$\text{Steady-state is reached in approximately five time constants.} \quad (6.1.4.2)$$

This sort of recursively dependent operation is characteristic of exponential functions. The equation for the capacitor's voltage charging curve is:

$$V_C(t) = E \left(1 - e^{-\frac{t}{\tau}} \right) \quad (6.1.4.3)$$

Where

$V_C(t)$ is the capacitor voltage at time t ,

E is the source voltage,

t is the time of interest,

τ is the time constant,

e (also written e) is the base of natural logarithms, approximately 2.718.

The dashed blue line shows the initial slope of current change. The solid blue curve shows the circulating current (and by extension of Ohm's law, the resistor voltage). The equation for this curve, which follows the general shape e^{-t} , is:

$$I(t) = \frac{E}{R} e^{-\frac{t}{\tau}} \quad (6.1.4.4)$$

and

$$V_R(t) = E e^{-\frac{t}{\tau}} \quad (6.1.4.5)$$

Once power is removed or bypassed, the stored charge on the capacitor will dissipate through any associated resistor(s) creating a discharge current which will end with the capacitor voltage drained back to zero. During the discharge phase, both the capacitor's voltage and current will follow the solid blue curve; Equations 6.1.4.4 and 6.1.4.5 being appropriate. The discharge time constant may be different from the charge times constant, depending on the associated resistances.

A precise derivation of the exponential charge/discharge equations is given in Appendix C.

✓ Example 8.4.1

Given the circuit of Figure 8.4.3, assume the switch is closed at time $t = 0$. Determine the charging time constant, the amount of time after the switch is closed before the circuit reaches steady-state, and the capacitor voltage at $t = 0$, $t = 50$ milliseconds and $t = 1$ second. Assume the capacitor is initially uncharged.

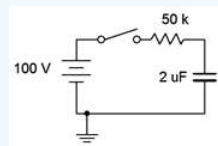


Figure 8.4.3 : Circuit for Example 8.4.1 .

First, the time constant:

$$\tau = RC$$

$$\tau = 50k\Omega 2\mu F$$

$$\tau = 100ms$$

Steady-state will be reached in five time constants, or 500 milliseconds. Therefore we know that $V_C(0) = 0$ volts and $V_C(1) = 100$ volts. To find $V_C(50ms)$ we simply solve Equation 6.1.4.3.

$$V_C(t) = E \left(1 - e^{-\frac{t}{\tau}} \right)$$

$$V_C(50ms) = 100V \left(1 - e^{-\frac{50ms}{100ms}} \right)$$

$$V_C(50ms) \approx 39.35V$$

This value can also be determined graphically from Figure 8.4.2 . The time of 50 milliseconds represents one-half time constant. Find this value on the horizontal axis and then track straight up to the solid red curve that represents the charging capacitor voltage. The point of intersection is at approximately 40% of the maximum value on the vertical axis. The maximum value here is the source voltage of 100 volts. Therefore the capacitor will have reached approximately 40% of 100 volts, or just about 40 volts.

Computer Simulation

The circuit of Figure 8.4.3 is entered into a simulator, as shown in Figure 8.4.4 . In order to reflect the notion of a time-varying circuit with a switch, the 100 volt DC voltage source has been replaced with a rectangular pulse voltage source. This source starts at 0 volts and then immediately steps up to 100 volts. It stays at this level for 500 milliseconds before dropping back to 0 volts.

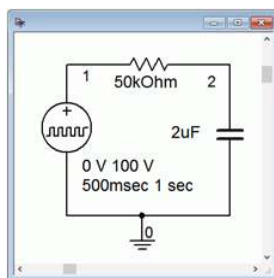


Figure 8.4.4 : Circuit of Figure 8.4.3 in a simulator.

A transient (i.e., time domain) simulation is run, plotting the capacitor voltage over time for the first 500 milliseconds. This is seen in Figure 8.4.5 . There are several items to note here. First, we see that the overall shape perfectly echoes the generic curve presented in Figure 8.4.2 . Second, we see that after the predicted five time constants, or 500 milliseconds, the capacitor voltage has plateaued, indicating steady-state. Third, at steady-state the capacitor voltage has virtually reached the maximum value set by the source, or 100 volts. Finally, at 50 milliseconds, we see that the capacitor voltage has reached roughly 40 volts, just as predicted.

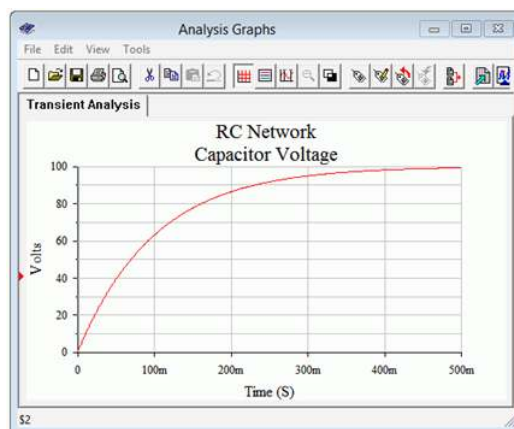


Figure 8.4.5 : Simulation results for the circuit of Figure 8.4.2 .

As mentioned previously, it is possible for a circuit to have different charge and discharge time constants. This could occur if a switch introduces or removes component(s) between the charge versus discharge phases. Further, because the capacitor is discharging, its current direction will be opposite to that of the charging current. KVL still must be satisfied, but because the capacitor is now behaving as a source, the magnitude of the discharge resistance's voltage must equal the capacitor voltage magnitude. Therefore, its curve will take the same shape (the solid blue curve of Figure 8.4.2). These issues will be illustrated in the following example.

✓ Example 8.4.2

For the circuit of Figure 8.4.6 , assume the capacitor is initially uncharged. At time $t = 0$ the switch contacts position 1. The switch is thrown to position 2 at time $t = 50$ milliseconds.

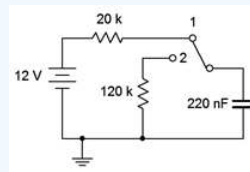


Figure 8.4.6 : Circuit for Example 8.4.2 .

Determine the charging time constant, the amount of time after the switch is closed before the circuit reaches steady-state, the maximum charging and discharging currents, and the capacitor voltage at $t = 0$, $t = 50$ milliseconds, $t = 90$ milliseconds, and $t = 1$ second.

We begin with the charge time constant:

$$\tau_{charge} = RC$$

$$\tau_{charge} = 20k\Omega 220nF$$

$$\tau_{charge} = 4.4ms$$

Steady-state will be reached in 5 times 4.4 milliseconds, or 22 milliseconds. The capacitor is initially uncharged, so $V_C(0) = 0$ volts. As the capacitor will have reached steady-state in 22 milliseconds, $V_C(50ms) = 12$ volts. The maximum charging current will occur at $t = 0$ when all of the 12 volt source drops across the 20 kΩ resistor, or 600 μamps, flowing left to right.

At 50 milliseconds the switch is thrown to position 2. The 12 volt source and 20 kΩ resistor are no longer engaged. At this point the capacitor has 12 volts across it, positive to negative, top to bottom. As the capacitor voltage cannot change instantaneously, the capacitor now acts as a voltage source and discharges through the 120 kΩ resistor. Note that the discharge current is flowing counterclockwise, the opposite of the charging current. The discharge time constant is:

$$\tau_{discharge} = RC$$

$$\tau_{discharge} = 120k\Omega 220nF$$

$$\tau_{discharge} = 26.4ms$$

The capacitor will fully discharge down to 0 volts in 5 time constants, or some 132 milliseconds after the switch is thrown to position 2. Thus steady-state occurs at $t = 182$ milliseconds. The maximum discharge current occurs the instant the switch is thrown to position 2 when all of the capacitor's 12 volts drops across the 120 kΩ resistor, yielding 100 μ amps, flowing top to bottom.

Clearly, at $t = 90$ milliseconds the capacitor is in the discharge phase. The capacitor's voltage and current during the discharge phase follow the solid blue curve of Figure 8.4.2 . The elapsed time for discharge is 90 milliseconds minus 50 milliseconds, or 40 milliseconds net. We can use a slight variation on Equation 6.1.4.5 to find the capacitor voltage at this time.

$$V_C(t) = Ee^{-\frac{t}{\tau}}$$

$$V_C(40ms) = 12V - e^{-\frac{40ms}{26.4ms}}$$

$$V_C(40ms) \approx 2.637V$$

The shape of the capacitor's voltage will appear somewhat like a rounded pulse, rising with a curve and then falling back to zero with a complementary curve (the red and then blue curves of Figure 8.4.2).

Basic single resistor-capacitor circuits prove to be fairly easy to solve given a little practice, but what if a more complex circuit is used? In this situation the section feeding the capacitor may be simplified using Thévenin's theorem to determine the effective source voltage and charging resistance. The circuit then reverts back to a simple RC network which may be solved directly.

If power is interrupted before the capacitor is fully charged, the equations presented previously may be used to determine the precise voltage(s) and current(s) reached. The capacitor will then behave as a voltage source and begin to discharge, its voltage curve following the blue plot line of Figure 8.4.2 , with its maximum voltage being what the capacitor charged to, not the associated driving voltage. The following example and simulations address these issues.

✓ Example 8.4.3

For this example we shall revisit the circuit of Example 8.3.1. The circuit is redrawn in Figure 8.4.7 for convenience. Assume the capacitor is initially uncharged.

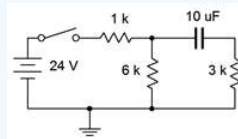


Figure 8.4.7 : Circuit for Example 8.4.3 .

Determine the charging time constant, the amount of time after the switch is closed before the circuit reaches steady-state, and the capacitor voltage at $t = 0$, 100 milliseconds, and 200 milliseconds. At 200 milliseconds, the switch is opened. Determine how long it takes for the capacitor to fully discharge and the voltage across the 6 kΩ resistor at $t = 275$ milliseconds (i.e., 75 milliseconds after the switch is opened).

The first step is to determine the Thévenin equivalent driving the capacitor. If we remove the capacitor and determine the open circuit voltage at those points, we see that it is just a voltage divider between the 24 volt source, the 6 kΩ resistor and the 1 kΩ resistor (the 3 kΩ resistor has no current through it and thus produces no voltage drop). This works out to 20.57 volts. The Thévenin resistance will be 3 kΩ in series with $1\text{ k}\Omega \parallel 6\text{ k}\Omega$, or roughly 3.857 kΩ. The equivalent charging circuit is drawn in Figure 8.4.8 .

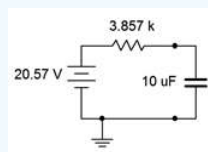


Figure 8.4.8 : Thévenin equivalent for the circuit of Figure 8.4.7 driving the capacitor.

We can now determine the charging time constant:

$$\tau_{charge} = RC$$

$$\tau_{charge} = 3.857\text{k}\Omega 10\mu\text{F}$$

$$\tau_{charge} = 38.57\text{ms}$$

Steady-state will be reached in 5 time constants, or 192.8 ms. Thus, we know that $V_C(0) = 0$ volts and $V_C(200\text{ms}) = 20.57$ volts. For the capacitor voltage at 100 milliseconds, we simply use the charge equation.

$$V_C(t) = E \left(1 - e^{-\frac{t}{\tau}} \right)$$

$$V_C(100\text{ms}) = 20.57\text{V} \left(1 - e^{-\frac{100\text{ms}}{38.57\text{ms}}} \right)$$

$$V_C(100\text{ms}) \approx 19.03\text{V}$$

For the discharge phase, we need to determine the time constant. With the voltage source removed, the capacitor will discharge through the now series combination of the 3 kΩ resistor and 6 kΩ resistor.

$$\tau_{discharge} = RC$$

$$\tau_{discharge} = 9\text{k}\Omega 10\mu\text{F}$$

$$\tau_{discharge} = 90\text{ms}$$

Steady-state will be reached 450 milliseconds later at $t = 650$ milliseconds. To find V_{6k} at $t = 275$ milliseconds, we can find the voltage across the capacitor and then perform a voltage divider between the $6\text{ k}\Omega$ and $3\text{ k}\Omega$ resistors. Remembering that $t = 275$ milliseconds is 75 milliseconds into the discharge phase, we have:

$$V_C(t) = Ee^{-\frac{t}{\tau}}$$

$$V_C(75\text{ms}) = 20.57\text{V} \left(1 - e^{-\frac{75\text{ms}}{90\text{ms}}}\right)$$

$$V_C(75\text{ms}) \approx 8.94\text{V}$$

Finally, this voltage splits between the $6\text{ k}\Omega$ and $3\text{ k}\Omega$ resistors. Using the voltage divider rule, we find:

$$V_{6k} = V_C \frac{R_x}{R_x + R_y}$$

$$V_{6k} = 8.94\text{V} \frac{6\text{k}\Omega}{6\text{k}\Omega + 3\text{k}\Omega}$$

$$V_{6k} = 5.96\text{V}$$

Computer Simulation

In order to verify the analysis of Example 8.4.3, the circuit of Figure 8.4.7 is entered into a simulator, as shown in Figure 8.4.9. In place of a DC source, a pulse generator is used to mimic the on-off nature of the switch. This starts at zero volts and then immediately jumps up to 24 volts. It stays at this level for 200 milliseconds before returning back to zero. This is sufficient time to check whether or not the capacitor voltage has reached steady-state (predicted to take 192.8 milliseconds).

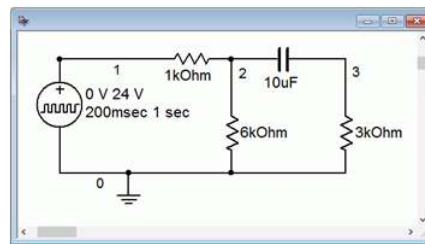


Figure 8.4.9 : Circuit of Figure 8.4.7 in a simulator.

A transient analysis is run on this circuit, plotting the capacitor voltage (i.e., the difference between the node 2 and node 3 voltages). The result is shown in Figure 8.4.10. This plot confirms nicely the charge phase of the capacitor. After approximately 200 milliseconds, the voltage has leveled out at just over 20 volts, precisely as predicted.

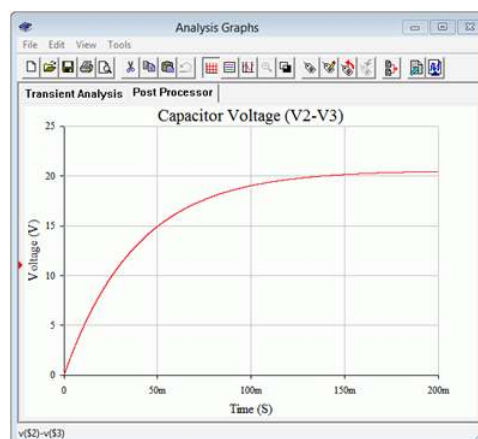


Figure 8.4.10 : Simulation results for the charge phase of the circuit of Figure 8.4.7.

What about the discharge phase? In order to investigate that portion, the simulation circuit is modified. The pulse voltage source is disconnected from the remainder of the circuit, just as it would be if the switch in Figure 8.4.7 had been opened again. Also, the capacitor is modified to have an initial voltage of 20.57 volts, the precise value it had reached after it attained steady-state. A second transient analysis is run, again plotting the capacitor voltage. The results of this simulation are shown in Figure 8.4.11. It is worth noting that the time axis is relative to the switch being opened, not the original timing. That is, the horizontal origin of 0 milliseconds corresponds to $t = 200$ milliseconds.

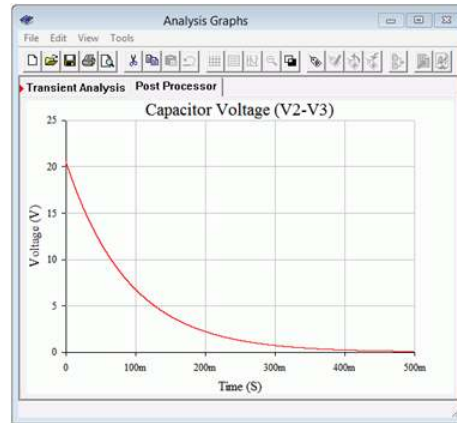


Figure 8.4.11 : Simulation results for the discharge phase of the circuit of Figure 8.4.7 .

Note that the time required to reach the new steady-state value of zero volts has stretched out to some 450 milliseconds after the switch is opened, precisely as predicted.

At this point, a fair question to ask is, “Couldn’t we leave the pulse source in place in order to investigate the discharge phase?” Although the pulse source does go back down to zero volts at $t = 200$ milliseconds, that’s not the same as opening the switch back in Figure 8.4.7 . If the source is still connected but producing zero volts, it becomes part of the Thévenin equivalent. As such, the $1\text{ k}\Omega$ resistor is back in the circuit, producing a discharge time constant identical to the charge time constant.

To prove the point, the simulation is run again. The pulse remains at 24 volts for 200 milliseconds and then jumps down to zero, as before. The simulation time is extended out to 400 milliseconds total, enough to see both the charge and discharge phases. Further, instead of just plotting the capacitor voltage; the voltages of the source (blue trace, node 1), the $6\text{ k}\Omega$ resistor (green trace, node 2) and the $3\text{ k}\Omega$ resistor (red trace, node 5) are plotted. The results are shown in Figure 8.4.12 .

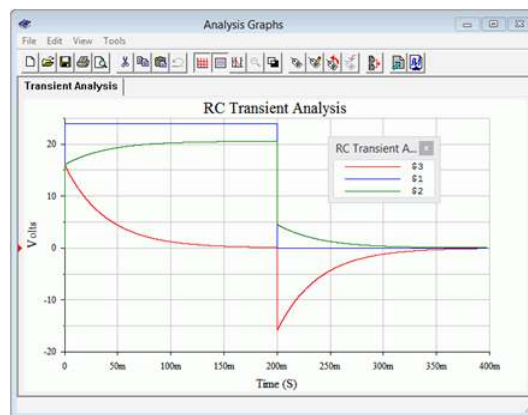


Figure 8.4.12 : Simulation results using pulse voltage source for discharge phase.

The first item to note is that steady-state appears to be reached in just under 200 milliseconds for both the charge and discharge phases, as expected. Second, note that the node 2 voltage (green) minus the node 3 voltage (red) starts at zero and winds up at a little over 20 volts at 200 milliseconds. This is, of course, the capacitor voltage, but what is interesting here is that this plot shows how the voltage across the $3\text{ k}\Omega$ resistor shrinks as the capacitor voltage grows, the sum equaling the node 2 voltage. This makes

perfect sense because, as the capacitor voltage increases, the current through it must be decreasing, and as this same current is flowing through the $3\text{ k}\Omega$ resistor, the resistor's voltage must also be decreasing due to Ohm's law.

The other interesting part of this plot is what happens at 200 milliseconds when the source goes back to zero. Note that the node 3 voltage immediately jumps to a negative value. This is because the voltage across the capacitor cannot change instantaneously. It must still have 20.57 volts across it the instant the source goes back to zero. In this situation, because the source is essentially a short, the capacitor winds up in series with the $3\text{ k}\Omega$ resistor and the parallel combination of the $1\text{ k}\Omega$ and $6\text{ k}\Omega$ resistors, or about $857\ \Omega$. Calculating the voltage divider between the $3\text{ k}\Omega$ and $857\ \Omega$ resistors with 20.57 volt source shows the $3\text{ k}\Omega$ resistor receiving approximately 16 volts. Further, the discharge current will be flowing out of the capacitor in a counterclockwise direction, meaning it flows from ground up through the $3\text{ k}\Omega$ resistor. Thus, we expect node 3 to be at approximately -16 volts, which is precisely what the plot indicates. How cool is that?

What if we didn't wait for steady-state? How would these plots change? Essentially, the trajectories of the curves would not change. After all, how would the circuit “know” that the switch would open early or the pulse would flip prematurely?

What happens is that the curves are followed to the point in time where the circuit is interrupted. From there, the next phase occurs with the present voltages as the starting points. To test this, the simulation is run yet again, but this time the source pulse width is shortened to just 50 milliseconds, well short of steady-state. The results of the simulation are shown in Figure 8.4.13 .

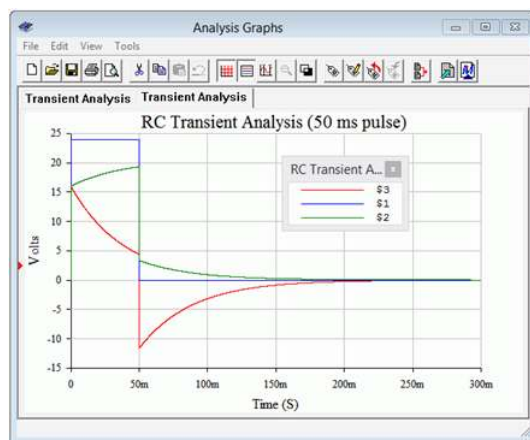


Figure 8.4.13 : Simulation results for interrupted discharge phase using pulse voltage source.

Comparing the plot of Figure 8.4.13 to that of Figure 8.4.12 shows that the two are identical up to 50 milliseconds. At that point, the input pulse returns to zero and the capacitor begins to discharge. The shapes and timings of the node 2 and node 3 voltages are the same as they were in Figure 8.4.12 , however, the amplitudes are reduced. This is because the capacitor did not have time to reach the steady-state voltage of 20.57 volts. In fact, it only reaches about 14.94 volts using Equation 6.1.4.3. Applying the voltage divider on this potential as before shows that the $3\text{ k}\Omega$ resistor should jump to approximately -11.6 volts, which is confirmed by the simulation.

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6.1.5: Summary

The capacitor is a device that is used to store electric charge. Capacitance, C , is measured in farads, F . The idealized device consists of two conductive plates separated by some distance, that space being filled by an insulating dielectric. Capacitance is directly proportional to the plate area and the dielectric's permittivity, and inversely proportional to the plate distance. Another important characteristic of the dielectric is its breakdown strength. Along with the plate spacing, this will establish the capacitor's voltage rating. The permittivity will also help to determine the capacitor's volumetric efficiency, a measure of how much capacitance can be achieved within a given volume. Non-ideal parameters include the ESR, or equivalent series resistance, which is ideally zero; and the effective parallel leakage resistance, ideally infinity. Absolute accuracy, temperature stability and similar parameters round out the distinguishing features of one kind of capacitor against another. When placed in parallel, capacitors add in the same manner as resistors in series. When placed in series, capacitors behave like resistors in parallel.

Perhaps the most important operational characteristic regarding capacitors is that voltage across a capacitor cannot change instantaneously. It will take some finite amount of time before the charge on the capacitor builds, leading to a predictable rise in voltage across it. Because of this, for DC circuits capacitors initially behave like shorts, but after sufficient time has passed, they behave like opens. The amount of time required to reach steady-state is five time constants, where one time constant is defined as the product of the circuit's effective resistance and its capacitance. The current charge curve is of the shape e^{-t} . The current starts at a maximum and eventually approaches zero as time passes. The corresponding voltage shape is of the form $1 - e^{-t}$. Here, the capacitor's voltage starts at zero and rises to some maximum value. The capacitor's voltage discharge curve effectively is swapped compared to the charge curve (e.g. voltage follows e^{-t}).

Review Questions

1. What are the physical characteristics of capacitors and how do they affect capacitance?
2. Define the voltage-current characteristic for capacitors.
3. What is meant by a capacitor's volumetric efficiency?
4. How do the permittivity and breakdown strength of the dielectric affect the overall capacitance and voltage rating?
5. How do capacitors combine when placed in series and how do they combine when placed in parallel?
6. Define the initial and steady-state behavior of capacitors.
7. Define time constant for an RC circuit.
8. Describe the charge and discharge characteristics of RC circuits.

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6.1.6: Exercises

Analysis

1. For the circuit shown in Figure 8.6.1 , determine the effective capacitance.

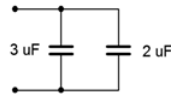


Figure 8.6.1

2. Determine the effective capacitance of the configuration shown in Figure 8.6.2 .

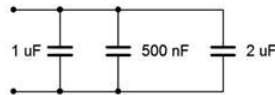


Figure 8.6.2

3. Given the capacitor network shown in Figure 8.6.3 , determine the effective value.



Figure 8.6.3

4. Determine the effective capacitance of network shown in Figure 8.6.4 .

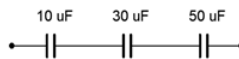


Figure 8.6.4

5. Determine the voltage across each capacitor for the circuit shown in Figure 8.6.5 .

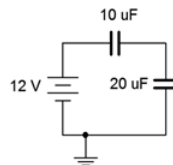


Figure 8.6.5

6. Determine the voltage across each capacitor for the circuit shown in Figure 8.6.6 .

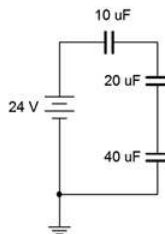


Figure 8.6.6

7. Determine the initial voltage across each component for the circuit shown in Figure 8.6.7 .

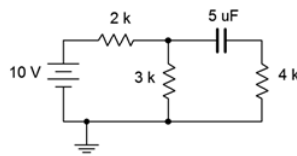


Figure 8.6.7

8. Given the network shown in Figure 8.6.7 , determine the steady-state voltage across each component.
9. For the circuit shown in Figure 8.6.8 , determine the capacitor voltage 3 microseconds after the power is switched on.

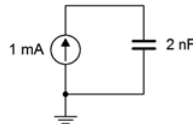


Figure 8.6.8

10. For the circuit shown in Figure 8.6.9 , determine the capacitor voltage 5 seconds after the power is switched on.

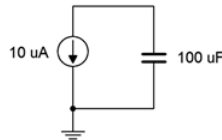


Figure 8.6.9

11. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 8.6.10 .

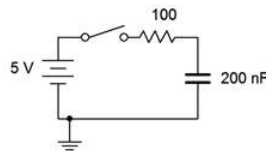


Figure 8.6.10

12. For the circuit shown in Figure 8.6.10 , determine the capacitor voltage and circulating current 20 microseconds and 100 milliseconds after the switch is thrown.
13. Given the circuit shown in Figure 8.6.11 , determine the capacitor voltage and circulating current 200 milliseconds and 10 seconds after the switch is thrown.

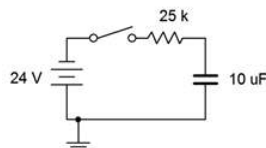


Figure 8.6.11

14. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 8.6.11 .
15. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 8.6.12 , switch position 1.

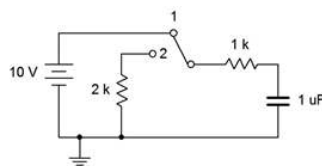


Figure 8.6.12

16. Determine the charge and discharge time constants for the circuit shown in Figure 8.6.13 .

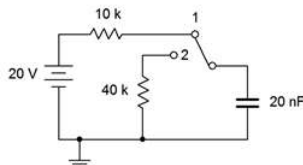


Figure 8.6.13

17. Given the circuit shown in Figure 8.6.12 , determine the capacitor voltage 10 milliseconds after the power is turned on. At this point, the switch is thrown to position 2. Determine how long it will take the capacitor to discharge to nearly zero volts.

18. For the circuit shown in Figure 8.6.13 , determine the capacitor voltage 400 microseconds after the power is turned on. At this point, the switch is thrown to position 2. Determine how long it will take the capacitor to discharge to nearly zero volts.

19. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 8.6.14 , switch position 1.

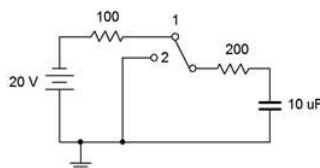


Figure 8.6.14

20. Given the circuit shown in Figure 8.6.14 , determine the capacitor voltage 12 milliseconds after the power is turned on. At this point, the switch is thrown to position 2. Determine how long it will take the capacitor to discharge to nearly zero volts.

Design

21. Given the circuit of Figure 8.6.10 , determine a new resistor value such that steady-state is reached in 2 milliseconds.

22. Given the circuit of Figure 8.6.11 , determine a new resistor value such that steady-state is reached in 5 seconds.

23. When an audio amplifier is turned on, the power surge can cause an audible pop from the loudspeaker. To prevent this, amplifiers often connect to the loudspeaker via a relay. The relay is energized to connect the loudspeaker once the output has settled, typically a few seconds after power is applied. This delay may be created via an RC network. Suppose the driving circuit is 5 volts and the relay trips at 4 volts. Further, the associated charging resistance is 10 kΩ. Determine the capacitance required to achieve a 2 second delay time.

Challenge

24. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 8.6.15 .

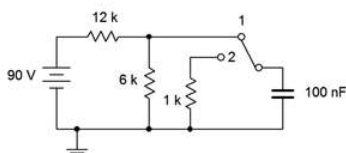


Figure 8.6.15

25. For the circuit shown in Figure 8.6.15 , determine the capacitor voltage 1 second after the power is turned on. At this point, the switch is thrown to position 2. Determine how long it will take the capacitor to discharge to nearly zero volts.

Simulation

26. Perform a transient analysis to verify the time to steady-state of Figure 8.6.10 (problem 11).
27. Perform a transient analysis to verify the time to steady-state of Figure 8.6.11 (problem 14).
28. Use a transient analysis to verify the design of problem 21.
29. Use a transient analysis to verify the design of problem 22.
30. Use a transient analysis to verify the operation of the circuit shown in Figure 8.6.15 as specified in problem 25. You may wish to do this as two separate simulations, one for each switch position, with the second position using a pre-charged capacitor.

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SECTION OVERVIEW

6.2: Inductors

Learning Objectives

After completing this chapter, you should be able to:

- Describe the theoretical and practical aspects of inductor construction.
- Describe the current-voltage characteristic behavior of inductors.
- Utilize component data sheets to determine operating characteristics of inductors.
- Determine the initial and steady-state equivalents of resistor-inductor networks.
- Determine the initial and steady-state equivalents of resistor-capacitor-inductor networks.
- Determine the transient response of basic RL networks.

[6.2.1: Introduction](#)

[6.2.2: Inductance and Inductors](#)

[6.2.3: Initial and Steady-State Analysis of RL Circuits](#)

[6.2.4: Initial and Steady-State Analysis of RLC Circuits](#)

[6.2.5: Transient Response of RL Circuits](#)

[6.2.6: Summary](#)

[6.2.7: Exercises](#)

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6.2.1: Introduction

This chapter introduces our third passive device, the inductor. Inductors are fundamentally different from both resistors and capacitors in terms of their construction and their operation. Inductors do, however, share certain broad traits with capacitors. First, they are energy storage devices. In the case of the inductor, energy is stored in a magnetic field, similar to the case of the capacitor which utilizes an electric field. Further, in the ideal case, inductors do not dissipate power. Also like capacitors, when inductors are placed in DC circuits they are not ohmic, meaning that their current-voltage characteristic does not respond to Ohm's law. Instead, their current-voltage characteristic is dynamic in nature. In some respects, though, their current-voltage behavior is opposite to the way in which capacitors behave, and thus they offer their own unique performance characteristics.

Inductors have a long history of use in electronic systems. In fact, one of the most common uses in the home is as an integral part of a typical loudspeaker system. They are used in modern switch-mode DC power supplies in products such as personal computers and televisions. In audio and communications systems they are used in filters and tuning circuits alongside capacitors. Like a capacitor, for any application that needs to smooth out a varying voltage, store energy or filter a signal; an inductor is a likely candidate.

Unfortunately, real-world inductors generally do not behave as close to their desired ideal operation as do realworld capacitors. The secondary effects of inductor construction limit their performance; perhaps the most notable factor being their potentially large equivalent series resistance. They are also susceptible to external magnetic fields which can introduce noise and interference, degrading signal quality. For these reasons, there are areas where, given a choice, capacitors would be preferred over inductors. But this is by no means a broad condemnation and there are areas where the use of inductors is essential. Beyond this, the very concept of inductance is important in that informs designers of the practical limits of performance of their circuits.

The concept of electromagnetic induction was first discovered by English scientist Michael Faraday in the early 19th century. He noticed that if he wrapped two wires around an iron ring and introduced a current in one of them, then a transient (shortlived) current would appear in the second coil of wire. He noticed a similar effect when he slid a bar magnet through a wire coil. Around the same time, American Joseph Henry discovered much the same independently of Faraday and performed considerable research in this area. In his honor, the unit of inductance, the henry (abbreviated H), is named after him. The symbol for inductance is L, named after physicist Heinrich Emil Lenz. Inductors are commonly referred to as coils or chokes, for reasons that will be apparent shortly

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6.2.2: Inductance and Inductors

To begin, we need to examine the interrelation between electric current and magnetic fields in a conductor. When a current passes through a conductor, such as a wire, a magnetic field is created around the conductor that is proportional to the strength of the current. This is illustrated in Figure 9.2.1 .

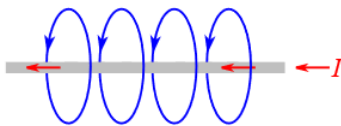


Figure 9.2.1 : Magnetic field around a conductor.

The magnetic field can be thought of as sets of concentric rings around the conductor, although for clarity only single loops are drawn in the Figure. The number of magnetic lines in a given area is known as the magnetic flux and is given the symbol Φ (the Greek letter phi). The unit of magnetic flux is the weber, Wb, named after Wilhelm Weber, a 19th century German physicist.

$$\text{Magnetic flux} \equiv \text{the number of magnetic lines enclosed in a given area.} \quad (6.2.2.1)$$

Note that the magnetic field runs the length of the conductor. The direction of the field lines follows the right hand rule: if you grasp the wire with your right hand such that your thumb is pointing in the direction of conventional current flow, then your fingers wrap in the direction of the magnetic field. This rule is illustrated in Figure 9.2.2 .



Figure 9.2.2 : Right hand rule. Image source (modified)

If we form the conductor into a loop, the field lines are corralled into the center of the loop. This is illustrated in Figure 9.2.3 . In this diagram it can be seen that the lines effectively collect in the center, going into the page.

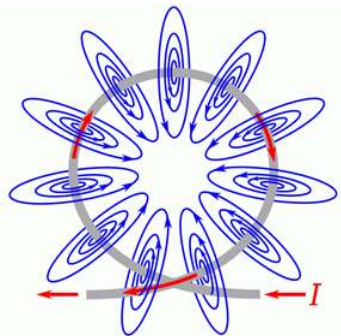


Figure 9.2.3 : Magnetic field around a loop.

The enhancement effect can be magnified by adding more loops in tandem. This is known as a solenoid and is shown in Figure 9.2.4 . It is the most basic form of an inductor.



Figure 9.2.4 : Solenoid.

The concentrating effect of the magnetic field is shown in Figure 9.2.5 . In this figure, the coil is shown from the side, as a cross-section of the individual loops. The dots inside the conductors indicate that the current is flowing toward you, out of the page; while the crosses indicate that the current is flowing into the page. The lines of flux exit out the right, loop around, and reenter from the left. Due to limited space, the entire loop for each line is not drawn, and it is important to remember that magnetic flux

lines do not end, but always create a loop. Further, although it is shown as a plane here, this field is three dimensional, with lines looping back into the page as well as in front of it.

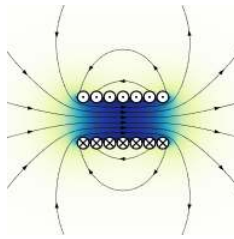


Figure 9.2.5 : Magnetic field in a solenoid. Image source

This is how electromagnets can be created¹. The north pole is the exiting end (right side) of Figure 9.2.5 while the south pole is the entering end (left side).

If the current changes, there will be a commensurate change in the magnetic field. Further, this change in the field will induce a current in the conductor that creates a magnetic field that opposes the original change in the field. This is known as Lenz's law. Alternately, it can be stated that the induced current caused by a changing magnetic field will oppose the change in the original current that created that change in the original magnetic field.

At this point we can offer a proper definition of the weber:

$$\begin{aligned} 1 \text{ weber} &\equiv \text{the magnetic flux that, acting on a single loop of a conductor,} \\ &\text{produces a potential of 1 volt if the flux is reduced to zero} \\ &\text{at an even rate over 1 second.} \end{aligned} \quad (6.2.2.2)$$

In magnetic circuits we are also interested in the magnetic flux density which is the magnetic flux per unit area. The symbol for flux density is B and has units of teslas (T), named after Nicola Tesla, the Serbo-Croatian-American engineer and inventor. One tesla is defined as one weber per square meter.

$$1 \text{ tesla} \equiv 1 \text{ weber/meter}^2 \quad (6.2.2.3)$$

To provide a reference, the magnetic flux density of the Earth near the equator is approximately $31 \mu\text{T}$, while the value of the voice coil gap in a loudspeaker is around 1 to 2 T, with medical MRI scanners being a little higher still.

Finally, we come to the definition of inductance and its unit, the henry:

$$\text{Inductance is a measure of the tendency of a conductor to oppose a change in the current flowing through it.} \quad (6.2.2.4)$$

$$1 \text{ henry} \equiv 1 \text{ weber/1 amp} \quad (6.2.2.5)$$

Unsurprisingly, the energy stored in the magnetic field of an inductor is proportional to the inductance. It is also proportional to the square of the current through the inductor.

$$W = \frac{1}{2} LI^2 \quad (6.2.2.6)$$

Where

W is the energy in joules,

L is the inductance in henries,

I is the current in amps.

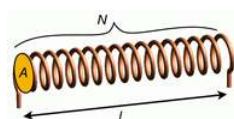


Figure 9.2.6 : Simple air-core inductor dimensions.

An inductor in its simplest form consists of a series of wire loops. These might be wound around an iron core, although a non-ferrous core might also be used. For a simple single layer inductor, such as the one drawn in Figure 9.2.6 , the inductance is described by the following formula:

$$L = \mu \frac{AN^2}{l} \quad (6.2.2.7)$$

Where

L is the inductance in henries,

μ is the permeability of the core material,

A is the cross sectional area of the coil,

N is the number of coils or turns,

l is the length of the coil.

Inductors may also be wound using multiple layers or around a toroidal core, and these designs utilize alternate formulas.

Inductor Styles and Packaging

Equation 6.2.2.7 indicates that, in order to achieve high inductance, we would like a core with high permeability, permeability being a measure of how easy it is to establish magnetic flux in said material. Substances such as iron or ferrite have a much greater permeability than air and are used commonly for cores. They do have a disadvantage in that they will saturate sooner than an air core, and this can lead to distortion.



Figure 9.2.7 : Electric bass guitar pickup.

Another approach is to pack as many turns as is possible within a given length. One way to do this is to minimize the thickness of the insulation around the wire². This can be achieved by using a thin enamel coating instead of the typical plastic insulation. A second method is to use a very fine wire. This leads to two problems, namely an undesirable increase in equivalent series resistance (known colloquially as coil resistance or R_{coil}), and limited current carrying capacity. All of these effects have to be balanced in order to achieve the best performance for a given application.

Commercial inductors range in value from a fraction of a nanohenry for small surface mount “chip” inductors up to several henries. Some devices exhibit large internal inductances even though they are not specifically used as inductors. One common example is a transformer. Another example is an electric guitar or bass pickup, such as the one shown in Figure 9.2.7 with its cover removed. Units such as this may be constructed of several thousand turns of very fine wire (typically AWG 41 to 44) and achieve inductances in excess of one henry.

A variety of inductors is shown in Figure 9.2.9 , all of which are of the through-hole type (surface mount inductors do not appear considerably different from their surface mount resistor and capacitor cousins).

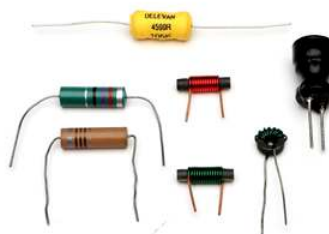


Figure 9.2.9 : A collection of inductors.

The two units toward the left are molded inductors and use a standard color code, similar to the ones used for resistors and capacitors. The unit at the top (yellow) is a high current inductor that features low R_{coil} . The three inductors in the center use obvious ferrite cores, two wound on straight cores and the third wound on a toroidal core. The unit to the right uses a high permeability material at the very top and is wrapped in a plastic sheath for protection. Variable inductors are also a possibility and can be made by using a ferrite core that can be slid within the coils, effectively changing the permeability of the core (part ferrite, part air).

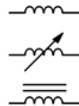


Figure 9.2.10 : Inductor schematic symbols (top-bottom): standard, variable, iron/ferrite core.

The schematic symbols for inductors are shown in Figure 9.2.10 . The standard symbol is at the top. The variable inductor symbol is in the middle and is a twolead device, somewhat reminiscent of the symbol for a rheostat. At the bottom is the symbol for an inductor with an iron, ferrite, or similar high permeability core. In general, like resistors, single inductors are not polarized and cannot be inserted into a circuit backwards. There are, however, special applications where multiple coils can be wound on a common core, and for these, the polarity of their interconnection can make a difference.

Inductor Data Sheet

A portion of an inductor data sheet is shown in Figure 9.2.12 . This page lists the available sizes of this particular model, each with corresponding quantities. We can see this model is available in inductance values ranging from 1 μH up to 100 mH. Tolerance of the smaller values is $\pm 10\%$ while values at and above 33 μH are at $\pm 5\%$. Q is the quality factor and is particularly important in AC circuits (higher being better), along with its associated frequency, f_Q . Continuing across we find I_R . This is the maximum rated current. For the smaller values, we find they can withstand in excess of 2 amps while the larger units can withstand only tens of milliamps.



RF chokes						B82144A
LBC series, 5.2 x 12 (mm)						
Characteristics and ordering codes						
L_R μH	Tolerance ¹⁾	Q_{min}	f_Q MHz	I_R mA	R_{max} Ω	$f_{res,min}$ MHz
1.0	$\pm 10\% \triangle K$	40	7.96	2200	0.08	200
1.5		40	7.96	2100	0.09	190
2.2		40	7.96	1900	0.11	140
3.3		40	7.96	1750	0.13	120
4.7		40	7.96	1600	0.16	100
6.8		40	7.96	1500	0.19	80
10	$\pm 5\% \triangle J$	60	2.52	1400	0.22	60
15		60	2.52	1250	0.28	20
22		50	2.52	1100	0.35	12
33		40	2.52	900	0.43	8.0
47		40	2.52	800	0.50	5.0
68		30	2.52	700	0.60	4.5
100	$\pm 5\% \triangle J$	50	0.796	600	0.70	3.5
150		50	0.796	500	0.90	3.0
220		50	0.796	400	1.60	2.4
330		50	0.796	330	1.90	2.0
470		40	0.796	280	2.50	1.5
680		30	0.796	240	2.80	1.3
1000	$\pm 5\% \triangle J$	60	0.252	200	3.80	1.2
1500		60	0.252	160	6.00	1.0
2200		60	0.252	120	9.00	0.8
3300		60	0.252	110	12.0	0.6
4700		60	0.252	90	20.0	0.5
6800		60	0.252	80	30.0	0.4
10000	$\pm 5\% \triangle J$	50	0.0796	60	42.0	0.35
15000		50	0.0796	50	68.0	0.30
22000		50	0.0796	40	120	0.26
33000		50	0.0796	35	150	0.22
47000		40	0.0796	30	230	0.18
68000		40	0.0796	25	290	0.15
100000		30	0.0796	20	420	0.12

Figure 9.2.12 : Inductor data sheet. Courtesy of TDK

Finally, we come to R_{max} . This is also known as R_{coil} . It represents the equivalent series resistance of the inductor. In general, smaller is better. For this model, it ranges from a fraction of an ohm to a few hundred ohms. This trend is typical of inductors; all else being equal, the larger the inductance, the larger the value of the associated series resistance. In many circuits, the value of R_{coil} cannot be ignored.

Inductors in Series and in Parallel

Suppose we take two identical inductors and place them in series. This effectively doubles both the length and the number of loops. From Equation 6.2.2.7 we can see that doubling both the number of loops and the length would double the inductance. This is because N^2 goes up by a factor of four which is then halved by the increased length. Consequently, inductors in series add values just like resistors in series. By extension, inductors in parallel behave like resistors in parallel. The equivalent of parallel inductors can be found by using either the product-sum rule or by taking the reciprocal of the sum of their reciprocals.

✓ Example 9.2.1

Find the equivalent inductance of the network shown in Figure 9.2.11 .

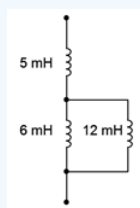


Figure 9.2.11 : Circuit for Example 9.2.1 .

The 6 mH and 12 mH inductors are in parallel. The equivalent value of the pair is:

$$L_{parallel} = \frac{L_2 L_3}{L_2 + L_3}$$

$$L_{parallel} = \frac{6mH \cdot 12mH}{6mH + 12mH}$$

$$L_{parallel} = 4mH$$

This combination is in series with the 5 mH inductor. Therefore the total equivalent inductance is 4 mH + 5 mH, or 9 mH.

Current-Voltage Relationship

The fundamental current-voltage relationship of the inductor is the mirror image of that of the capacitor:

$$v = L \frac{di}{dt} \quad (6.2.2.8)$$

This states that the voltage across the inductor is a function of how quickly the current is changing. If the current is not changing (i.e., in steady-state), then the voltage across the inductor is zero. In this case, the inductor behaves like a short, or more accurately, like its R_{coil} value. In contrast, during a rapid initial current change, the inductor voltage can be large, and thus the inductor behaves like an open.

If we rearrange Equation 6.2.2.8 and solve for the rate of change of current, we find that:

$$\frac{di}{dt} = \frac{v}{L} \quad (6.2.2.9)$$

Thus if an inductor is fed by a constant voltage source, the current will rise at a constant rate equal to v/L . For example, considering the circuit in Figure 9.2.11 , we see a voltage source feeding a single inductor. If we were to plot the inductor's current over time, we would see something like the graph of Figure 9.2.12 .

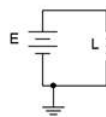


Figure 9.2.11 : Inductor with voltage source.

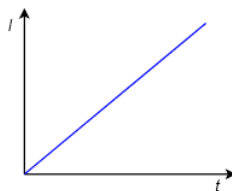


Figure 9.2.12 : Inductor current versus time.

As time progresses, the current through the inductor increases, flowing from top to bottom. With a theoretically perfect inductor and source, this would continue as long as the circuit was energized. In reality, this line would either begin to deflect horizontally as the source reached its limits, or the inductor would fail once its maximum current or power handling was reached. The slope of this line is dictated by the size of the applied voltage source and the inductance.

✓ Example 9.2.2

Determine the rate of change of current through the inductor in the circuit of Figure 9.2.13 . Also determine the inductor's current 10 microseconds after power is switched on.

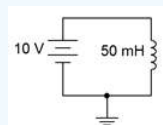


Figure 9.2.13 : Circuit for Example 9.2.2 .

From Equation 6.2.2.9, the rate of change of current is:

$$\begin{aligned}\frac{di}{dt} &= \frac{v}{L} \\ \frac{di}{dt} &= \frac{10V}{50mH} \\ \frac{di}{dt} &= 200A \text{ per second}\end{aligned}$$

In other words, for every second, the current rises another 200 amps. Thus, after just 10 microseconds it will have risen to 200 A/s times 10 μ s, or 2 mA.

Equation 6.2.2.8 is key to understanding the behavior of inductors. As noted previously, if an inductor is driven by a fixed voltage source and ignoring R_{coil} , the current through it rises at the constant rate of v/L . This change in current through the inductor is not limitless. An instantaneous change requires that di/dt is infinite, and thus, the voltage driving the inductor would also have to be infinite, which is a clear impossibility. Therefore we can state a particularly important characteristic of capacitors:

$$\text{The current through an inductor cannot change instantaneously.} \quad (6.2.2.10)$$

This observation will be central to analyzing the operation of inductors in DC circuits.

References

¹Truly one of the coolest inventions of all time: a magnet with an on/off switch.

²The wound wire must be insulated otherwise each loop will short to the loops next to it and we'd be left with a tube instead of a series of loops.

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6.2.3: Initial and Steady-State Analysis of RL Circuits

When analyzing resistor-inductor circuits, remember that current through an inductor cannot change instantaneously as this would require an infinite voltage source. When a circuit is first energized, the current through the inductor will still be zero, which is characteristic of opens. Once at steady-state, the current has leveled out and therefore the voltage across the inductor will approach zero, which is characteristic of shorts. Thus, we can state the general behavior of inductors at the beginning and ending of the charge cycle:

For DC analysis, initially inductors appear as opens. (6.2.3.1)

At steady-state, inductors appear as shorts. (6.2.3.2)

This is the opposite of what was seen with capacitors. For example, in the circuit of Figure 9.3.1, initially L is open, leaving us with R_1 and R_2 in series with the source, E . At steady-state, L shorts out, leaving R_1 in series with the parallel combination of R_2 and R_3 . All practical inductors will exhibit some internal resistance, so it is often best to think of an inductor as an ideal inductance with a small resistance (R_{coil}) in series with it.

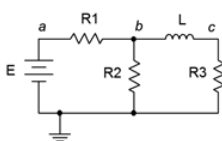


Figure 9.3.1 : Basic RL circuit.

✓ Example 9.3.1

Assuming the initial current through the inductor is zero in the circuit of Figure 9.3.2, determine the voltage across the $2\text{ k}\Omega$ resistor when power is applied and after the circuit has reached steady-state. Draw each of the equivalent circuits.

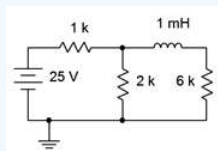


Figure 9.3.2 : Circuit for Example 9.3.1 .

First, we'll redraw the circuit for the initial-state equivalent. To do so, open the inductor. The new equivalent is shown in Figure 9.3.3. By opening the inductor, the $6\text{ k}\Omega$ resistor has been removed from the circuit and sees no voltage. What we are left with is a voltage divider between the source and the $1\text{ k}\Omega$ and $2\text{ k}\Omega$ resistors.

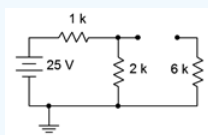


Figure 9.3.3 : Initial-state equivalent of the circuit of Figure 9.3.2 .

Using the voltage divider rule,

$$V_{2k} = E \frac{R_x}{R_x + R_y}$$

$$V_{2k} = 25V \frac{2k\Omega}{2k\Omega + 1k\Omega}$$

$$V_{2k} \approx 16.67V$$

For steady-state, we redraw using a short in place of the inductor, as shown in Figure 9.3.4. Here we have another voltage divider, this time between the $1\text{ k}\Omega$ resistor and the parallel combination of $2\text{ k}\Omega$ and $6\text{ k}\Omega$, or $1.5\text{ k}\Omega$.

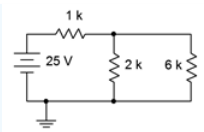


Figure 9.3.4 : Steady-state equivalent of the circuit of Figure 9.3.2 .

$$V_{2k} = E \frac{R_x}{R_x + R_y}$$

$$V_{2k} = 25V \frac{1.5k\Omega}{1.5k\Omega + 1k\Omega}$$

$$V_{2k} = 15V$$

Computer Simulation

To verify the results of Example 9.3.1 , the circuit is entered into a simulator as shown in Figure 9.3.5 . A DC operating point analysis is run and the results are shown in Figure 9.3.6 .

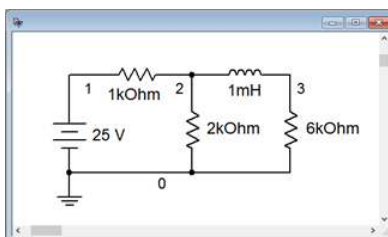


Figure 9.3.5 : Circuit of Figure 9.3.2 in a simulator.

The steady-state potential at node 2 corresponds to the voltage across the 2 kΩ resistor and agrees with the theoretical calculation of 15 volts. Note that node 3 is also 15 volts, indicating that the steady-state voltage across the inductor is zero, meaning it is behaving as a short, exactly as expected.

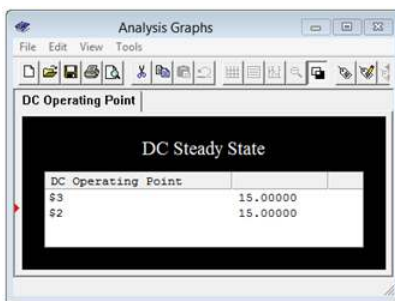


Figure 9.3.6 : Simulation results for the circuit of Figure 9.3.2 .

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6.2.4: Initial and Steady-State Analysis of RLC Circuits

When analyzing resistor-inductor-capacitor circuits, remember that capacitor voltage cannot change instantaneously, thus, initially, capacitors behave as a short circuit. Once the capacitor has been charged and is in a steady-state condition, it behaves like an open. This is opposite of the inductor. As we have seen, initially an inductor behaves like an open, but once steady-state is reached, it behaves like a short. For example, in the circuit of Figure 9.4.1, initially L is open and C is a short, leaving us with R_1 and R_2 in series with the source, E . At steady-state, L shorts out both C and R_2 , leaving all of E to drop across R_1 . For improved accuracy, replace the inductor with an ideal inductance in series with the corresponding R_{coil} value. Similarly, practical capacitors can be thought of as an ideal capacitance in parallel with a very large (leakage) resistance.

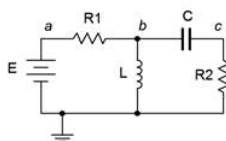


Figure 9.4.1 : Basic RLC circuit.

✓ Example 9.4.1

Assuming the initial current through the inductor is zero and the capacitor is uncharged in the circuit of Figure 9.4.2, determine the current through the $2\text{ k}\Omega$ resistor when power is applied and after the circuit has reached steady-state. Draw each of the equivalent circuits.

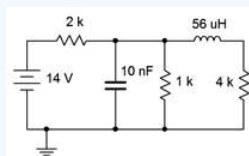


Figure 9.4.2 : Circuit for Example 9.4.1 .

For the initial-state equivalent we open the inductor and short the capacitor. The new equivalent is shown in Figure 9.4.3 . The shorted capacitor removes everything to its right from the circuit. All that's left is the source and the $2\text{ k}\Omega$ resistor.

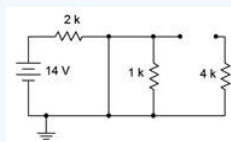


Figure 9.4.3 : Initial-state equivalent of the circuit of Figure 9.4.2 .

We can find the current through the $2\text{ k}\Omega$ resistor using Ohm's law.

$$I_{2k} = \frac{E}{R}$$

$$I_{2k} = \frac{14V}{2k\Omega}$$

$$I_{2k} = 7mA$$

Steady-state is redrawn in Figure 9.4.4, using a short in place of the inductor, and an open for the capacitor. We are left with a resistance of $2\text{ k}\Omega$ in series with the parallel combination of $1\text{ k}\Omega$ and $4\text{ k}\Omega$, or $2.8\text{ k}\Omega$ in total.

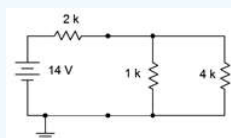


Figure 9.4.4 : Steady-state equivalent of the circuit of Figure 9.4.2 .

$$I_{2k} = \frac{E}{R}$$

$$I_{2k} = \frac{14V}{2.8k\Omega}$$

$$I_{2k} = 5mA$$

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6.2.5: Transient Response of RL Circuits

The transient response of RL circuits is nearly the mirror image of that for RC circuits. To appreciate this, consider the circuit of Figure 9.5.1 .

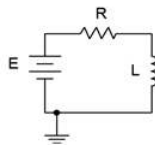


Figure 9.5.1 : RL circuit for transient response analysis.

Again, the key to this analysis is to remember that inductor current cannot change instantaneously. When power is first applied, the circulating current must remain at zero. Therefore no voltage drop is produced across the resistor, and by KVL, the voltage across the inductor must equal the source, E . This establishes the initial rate of change of current via Equation 9.2.9 ($di/dt = E/L$) and is represented by the dashed red line in the graph of Figure 9.5.2 . As the current starts to increase, the voltage drop across the resistor begins to increase. This reduces the voltage available for the inductor, thus slowing the rate of change of current. This is depicted by the solid red curve on the graph. Meanwhile, the solid blue curve represents the decreasing inductor voltage. Thus, in the RL circuit, the inductor's voltage curve echoes the RC circuit's current curve (or resistor voltage curve), and the RL current curve echoes the RC circuit's capacitor voltage curve.

The curves presented in Figure 9.5.2 are identical to those presented in Chapter 8 when we discussed capacitors. They are reproduced here for your convenience.

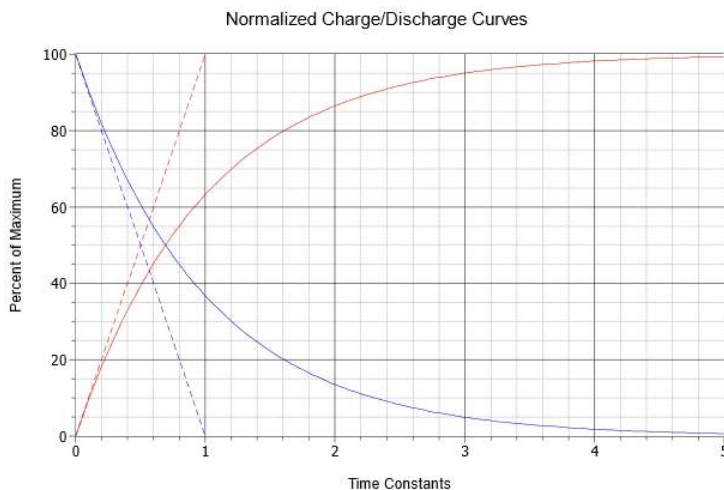


Figure 9.5.2 : Normalized charge and discharge curves.

As noted before, the rate of current change versus time is equal to v/L , and therefore in this case, E/L . If the initial rate of change were to continue unabated, the maximum (steady-state) current, E/R , would be reached in L/R seconds¹. Therefore the time constant for an RL circuit is:

$$\tau = \frac{L}{R} \quad (6.2.5.1)$$

Once again, five constants will achieve steady-state.

Following the prior work on capacitors, the relevant equations for the RL circuit can be shown to be²:

$$V_L(t) = E\epsilon^{-\frac{t}{\tau}} \quad (6.2.5.2)$$

$$V_R(t) = E\left(1 - \epsilon^{-\frac{t}{\tau}}\right) \quad (6.2.5.3)$$

$$I(t) = \frac{E}{R} \left(1 - e^{-\frac{t}{\tau}}\right) \quad (6.2.5.4)$$

Where

$V_L(t)$ is the inductor voltage at time t ,

$V_R(t)$ is the resistor voltage at time t ,

$I(t)$ is the current at time t ,

E is the source voltage,

R is the series resistance,

t is the time of interest,

τ is the time constant,

e (also written ϵ) is the base of natural logarithms, approximately 2.718.

Time for an example.

✓ Example 9.5.1

Given the circuit of Figure 9.5.3, assume the switch is closed at time $t = 0$. Determine the charging time constant, the amount of time after the switch is closed before the circuit reaches steady-state, and the inductor voltage and current at $t = 0$, $t = 2$ microseconds and $t = 1$ millisecond. Assume the inductor is initially uncharged.

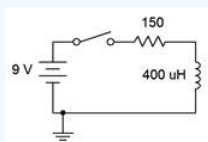


Figure 9.5.3 : Circuit for Example 9.5.1 .

First, the time constant:

$$\begin{aligned} \tau &= \frac{L}{R} \\ \tau &= \frac{400\mu H}{150\Omega} \\ \tau &\approx 2.667\mu s \end{aligned}$$

Steady-state will be reached in five time constants, or approximately 13.33 microseconds. Thus we know that $V_L(0) = 9$ volts and $V_L(1ms) = 0$ volts. Because the inductor is an open initially, $I_L(0) = 0$ amps. At $I_L(1 ms)$, the circuit is in steady-state and the inductor acts like a short. Therefore, all of the 9 volt source drops across the 150Ω resistor, for 60 mA.

To find $V_L(2 \mu s)$ we simply solve Equation 6.2.5.2.

$$\begin{aligned} V_L(t) &= E e^{-\frac{t}{\tau}} \\ V_L(2\mu s) &= 9V e^{-\frac{2\mu s}{2.667\mu s}} \\ V_L(2\mu s) &\approx 4.251V \end{aligned}$$

This value can also be determined graphically from Figure 9.5.2 . The time of 2 microseconds represents 75% of a time constant. Find this value on the horizontal axis and then track straight up to the solid blue curve that represents the charging inductor voltage. The point of intersection is right around 47% of the maximum value on the vertical axis. The maximum value here is the source voltage of 9 volts. Therefore the inductor will have reached approximately 47% of 9 volts, or just over 4.2 volts.

The current can be found in a similar manner using Equation 6.2.5.4.

$$I_L(t) = \frac{E}{R} \left(1 - e^{-\frac{t}{\tau}}\right)$$

$$I_L(2\mu s) = \frac{9V}{150\Omega} \left(1 - e^{-\frac{2\mu s}{2.667\mu s}}\right)$$

$$I_L(2\mu s) = 60mA \left(1 - e^{-0.75}\right)$$

$$I_L(2\mu s) = 31.66mA$$

Computer Simulation

To verify our analysis, the circuit of Figure 9.5.3 is entered into a simulator, as shown in Figure 9.5.4 . In order to reflect the notion of a time-varying circuit with a switch, the 9 volt DC voltage source has been replaced with a rectangular pulse voltage source. This source starts at 0 volts and then immediately steps up to 9 volts. It stays at this level for 20 microseconds before dropping back to 0 volts.

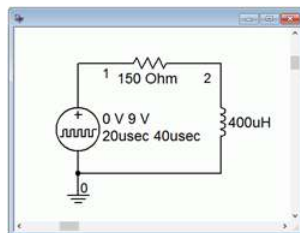


Figure 9.5.4 : The circuit of Figure 9.5.3 in a simulator.

The results of a transient analysis are shown in Figure 9.5.5 . The waveform shown tracks the inductor's voltage at node 2 with respect to ground.

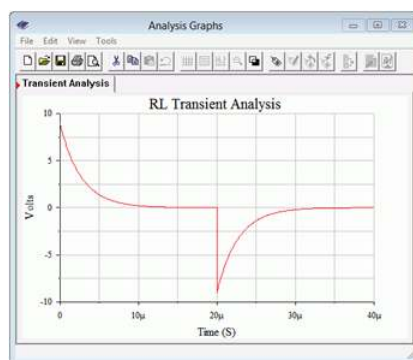


Figure 9.5.5 : Simulation results for the circuit of Figure 9.5.3 .

We can see that the voltage starts at 9 volts as expected. It then falls back to zero and is at steady-state in less than 15 microseconds, just as predicted. At 20 microseconds, the pulse source returns to zero volts. At this instant, the current through the inductor must still be the steady-state current of 60 milliamps. This current will still be flowing in a clockwise direction, thus it will produce a 9 volt drop across the 150 Ω resistor with a + to - polarity from left to right. This effectively places node 2 negative with respect to ground. The result is that the polarity of the inductor's voltage flips, with the inductor now acting as a short-lived source. We see this on the transient analysis as a negative 9 volt spike. The discharge time constant is identical to the charge constant, and thus we see the inductor's voltage fall back to zero in the same amount of time.

✓ Example 9.5.2

Given the circuit of Figure 9.5.6 , find V_L at $t = 1$ microsecond after the circuit is energized. Assume the inductor is initially uncharged.

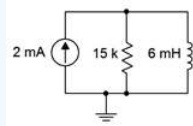


Figure 9.5.6 : Circuit for Example 9.5.2 .

First, the time constant:

$$\tau = \frac{L}{R}$$

$$\tau = \frac{6mH}{15k\Omega}$$

$$\tau = 400ns$$

Steady-state will be reached in five time constants, or 2 microseconds, at which point the inductor voltage will be zero as it will be behaving as a short. In contrast, as the inductor is initially an open ($I_L(0) = 0$), all of the current from the source will flow into the 15 kΩ resistor, producing 30 volts across this parallel network. Therefore, we can state that $V_L(0) = 30$ volts and $V_L(2 \mu s) = 0$ volts, defining the extremes. In order to find $V_L(1 \mu s)$, we can use Equation 6.2.5.2.

$$V_L(t) = Ee^{-\frac{t}{\tau}}$$

$$V_L(1\mu s) = 30Ve^{-\frac{1\mu s}{0.4\mu s}}$$

$$V_L(1\mu s) \approx 2.463V$$

There are a few different ways to crosscheck this value. For starters, we can determine the inductor current using a slight modification of Equation 6.2.5.4 (the current source value is used in place of E/R as the equation effectively requires the maximum or steady-state current).

$$I_L(t) = I(1 - e^{-\frac{t}{\tau}})$$

$$I_L(1\mu s) = 2mA(1 - e^{-\frac{1\mu s}{0.4\mu s}})$$

$$I_L(1\mu s) = 1.836mA$$

The inductor voltage of 2.463 volts would also have to appear across the parallel 15 kΩ resistor. This produces 2.463 V / 15 kΩ, or 0.164 mA of resistor current. By KCL, the remainder of the 2 mA source current must be flowing down through the inductor. This yields a net inductor current of 2 mA – 0.164 mA, or 1.836 mA, verifying our prior result.

Example 9.5.2 also reinforces the concept of the time constant being inversely proportional to the resistance, rather than directly proportional as in the RC case. In the circuit of Figure 9.5.6 , it should be obvious that the larger the resistance value, the larger the resulting initial-state voltage. From Equation 9.2.9 it can be seen that if the voltage across the inductor is increased, then the initial rate of change of current with respect to time will increase, and that implies a shorter time constant.

For more complex circuits, Thévenin's theorem may be used in order to determine the effective source voltage and charging resistance. As we saw with RC circuits, it's also possible that the discharge resistance may be considerably different from the charging resistance. In such a case, the charge and discharge curves can be highly asymmetric in both time and amplitude. Generally, the larger the discharge resistance is when compared to the charge resistance, the larger in voltage and the shorter in time the discharge spike will be (think in terms of the area under the curve staying constant).

✓ Example 9.5.3

Assume the initial current through the inductor is zero in Figure 9.5.7 . Determine the time constant. Also, determine the inductor voltage and the voltage across the 6 kΩ resistor 200 nanoseconds after the switch is closed.

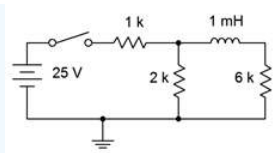


Figure 9.5.7 : Circuit for Example 9.5.3 .

This circuit is based on the circuit presented in Figure 9.3.2 as used in Example 9.3.1. In that analysis it was discovered that the steady-state voltage for the 6 kΩ and 2 kΩ resistors was 15 volts, the pair being in parallel. Further, the initial voltage across the 2 kΩ resistor and the inductor was 16.67 volts and for the 6 kΩ resistor, 0 volts.

For the Thévenin circuit, the open circuit voltage at the inductor would be the potential across the 2 kΩ resistor, which is obtained from a voltage divider between it and the 1 kΩ resistor, or 16.67 volts. The equivalent resistance is obtained by shorting the voltage source which leaves the 1 kΩ and 2 kΩ resistors in parallel, which is then in series with the 6 kΩ resistor, yielding approximately 6.667 kΩ. The equivalent is shown in Figure 9.5.8 .

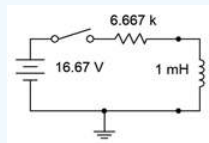


Figure 9.5.8 : Thévenin equivalent of the circuit of Figure 9.5.7 driving the inductor.

Immediately, we can see that the initial-state voltage across the inductor is confirmed in the equivalent circuit. We can now determine the time constant.

$$\tau = \frac{L}{R}$$

$$\tau = \frac{1mH}{6.667k\Omega}$$

$$\tau = 150ns$$

Steady-state will be reached in 750 nanoseconds. To find the inductor voltage we can use Equation 6.2.5.2.

$$V_L(t) = E\epsilon^{-\frac{t}{\tau}}$$

$$V_L(200ns) = 16.67V\epsilon^{-\frac{200ns}{150ns}}$$

$$V_L(200ns) \approx 4.39V$$

Referring back to the original circuit, in order to determine the voltage across the 6 kΩ resistor we can find the current through it and use Ohm's law. The current would be the same as the inductor's current as the two are in series. Thus, Equation 6.2.5.4 would do the trick.

$$I_L(t) = \frac{E}{R} (1 - \epsilon^{-\frac{t}{\tau}})$$

$$I_L(200ns) = \frac{16.67V}{6.667k\Omega} (1 - \epsilon^{-\frac{200ns}{150ns}})$$

$$I_L(200ns) = 2.5mA (1 - \epsilon^{-1.333})$$

$$I_L(200ns) \approx 1.841mA$$

And finally,

$$V_{6k}(200ns) = IR$$

$$V_{6k}(200ns) = 1.841mA \cdot 6k\Omega$$

$$V_{6k}(200ns) \approx 11.05V$$

Further, the voltage across the 2 k Ω resistor must be the sum, or approximately 15.44 volts.

Computer Simulation

The results of Example 9.5.3 are crosschecked in a simulator. Once again the circuit is built using a pulse generator, as shown in Figure 9.5.9 .

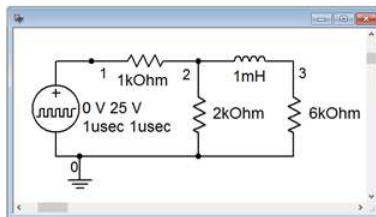


Figure 9.5.9 : Circuit of Figure 9.5.7 in a simulator.

A transient analysis is run out to 1 microsecond which is modestly into steady-state. Node voltages 2 and 3 are plotted, as shown in Figure 9.5.10 . The initial voltage across the 2 k Ω resistor (node 2) is as predicted, approximately 16.7 volts, and falls to 15 volts at steady-state, approximately 750 nanoseconds later. The voltage across the 6 k Ω resistor (node 3) starts at zero volts and also winds up at 15 volts in steadystate, just as predicted. Further, note that the predicted voltages across the 2 k Ω and 6 k Ω resistors at 200 nanoseconds are verified.

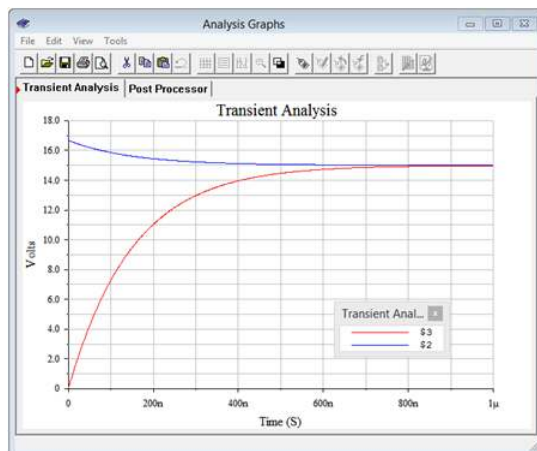


Figure 9.5.10 : Transient analysis simulation of the circuit of Figure 9.5.7 .

The voltage across the inductor is node 2 minus node 3. This differential is plotted separately in Figure 9.5.11 . The expected initial, steady-state and 200 nanosecond voltages are as predicted.

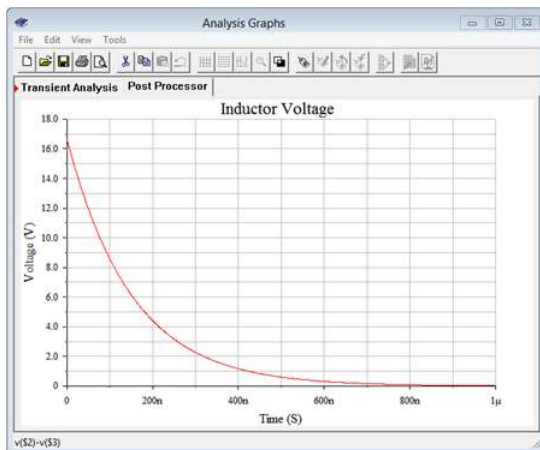


Figure 9.5.11 : Simulation of the inductor voltage versus time for the circuit of Figure 9.5.7 .

One very important observation is that if an RL circuit is abruptly altered or opened, very large voltage spikes may occur. This is due to the fact that inductor current cannot change instantaneously. If the circuit is opened, the open represents a very large resistance. Ohm's law indicates that the inductor current times this very large resistance may produce a very large voltage across the new open. In fact, the potential may be sufficient to cause a spark or arc. Note that because the current cannot change instantaneously (both magnitude and direction), the inductor now behaves as a voltage source of very high magnitude and with reverse polarity. This phenomenon is used to create the ignition spark in internal combustion engines. In short, the ignition coil is charged, creating some current flow. The circuit is then interrupted leaving just the coil in series with the spark plug, the spark plug being little more than a precisely sized gap between two electrodes. This results in a large voltage being developed across the spark plug gap, typically in the neighborhood of 20,000 volts, which is sufficient to create a small arc (i.e., the spark) that then ignites the air-fuel mixture in the piston.

An example of producing a discharge voltage spike that is considerably larger than the source voltage can be illustrated with the circuit of Figure 9.5.12 . We shall assume that the inductor is initially uncharged when power is applied, and that the switch is in position 1. In this case, the circuit consists of just the 12 volt source, the 2.2 k Ω resistor, and the inductor. The circuit reaches steady-state in roughly 227 nanoseconds. At that point the inductor behaves as a short, leaving the full 12 volt source to drop across the 2.2 k Ω resistor. This produces a clockwise current of approximately 5.455 mA.

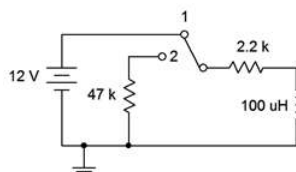


Figure 9.5.12 : Circuit illustrating large discharge voltage spike.

If we now move the switch to position 2, this current must be maintained because the current through the inductor cannot change instantaneously. The new discharge resistance is now the series combination of the two resistors, or 49.2 k Ω . Ohm's law and KVL dictate that the resulting inductor voltage must be 49.2 k Ω times 5.455 mA, or just beyond -268 volts. This potential is negative because the clockwise current is flowing up through the 47 k Ω resistor, producing a drop + to - from ground up. The increased resistance also shortens the time constant and now steady-state will be reached in only 10.1 nanoseconds. Thus, we see a much larger magnitude spike (over twenty times that of the source voltage) with a much shorter time duration (less than one-twentieth of the charge time).

Depending on the kind of switch that is used, things can be even more extreme than what has been just described. Switches come in two basic varieties: make-before-break and break-before-make. The former makes contact with the second position before it breaks contact with the first position, while the latter does the opposite. The behavior just described assumes that a make-before-break switch is being used. In contrast, if a break-before-make switch is used, we'd see a drastically different result.

Let us pick up back at steady-state with 5.455 mA flowing through the inductor. We now throw the switch to position 2. This new switch breaks contact with the wire leading back to voltage source prior to it making contact with the 47 k Ω resistor. For a short instant of time the switch is not making contact with anything and the resulting resistance in the loop is determined by the air gap between the switch contacts. Even if this was a mere 10 M Ω , the resulting potential would be over 50,000 volts. This will almost certainly create a spark and we will have inadvertently recreated the spark plug scenario. Hopefully, there are no combustible gases nearby.

References

¹Which is to say, E/L amps per second times L/R seconds yields E/R amps.

²See also Appendix C.

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6.2.6: Summary

The inductor is a device that stores energy in the form of a magnetic field. Inductance, L , is measured in henries, H . The idealized device consists of several loops or coils of wire. These may or may not be wrapped around a magnetic core material. Inductance is directly proportional to the permeability of the core material and the cross sectional area of the loops, and inversely proportional to the length of the coil. It is also proportional to the square of the number of loops. The most important non-ideal parameter is R_{coil} , or equivalent coil resistance. Ideally, this value is zero. Absolute accuracy, temperature stability and similar parameters round out the distinguishing features of one kind of inductor against another. When placed in series, inductors add in the same manner as resistors in series. When placed in parallel, inductors combine like resistors in parallel.

Perhaps the most important operational characteristic regarding inductors is that current through an inductor cannot change instantaneously. It will take some finite amount of time before the magnetic field reacts, leading to a predictable rise in current through it. Because of this, for DC circuits inductors initially behave like opens, but after sufficient time has passed, they behave like shorts. The amount of time required to reach steady-state is five time constants, where one time constant is defined as the inductance divided by the circuit's effective resistance. The current charge curve is of the shape $1 - e^{-t}$. The inductor's current starts at zero and rises to some maximum value. The corresponding voltage shape is of the form e^{-t} . Here, the voltage starts at a maximum and eventually approaches zero as time passes.

Review Questions

1. What are the physical characteristics of inductors and how do they affect inductance?
2. Define the voltage-current characteristic for inductors.
3. What is R_{coil} ?
4. How do inductors combine when placed in series? How do they combine when placed in parallel?
5. Define the initial and steady-state behavior of inductors.
6. Define time constant for an RL circuit.
7. How do the charge and discharge characteristics of RL circuits compare to those of RC circuits?

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6.2.7: Exercises

Analysis

1. For the circuit shown in Figure 9.7.1 , determine the effective inductance.

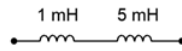


Figure 9.7.1

2. Determine the effective inductance of the network shown in Figure 9.7.2 .

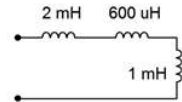


Figure 9.7.2

3. Given the inductor network shown in Figure 9.7.3 , determine the effective value.

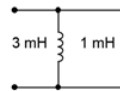


Figure 9.7.3

4. Determine the effective inductance of network shown in Figure 9.7.4 .

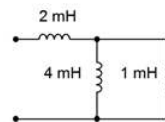


Figure 9.7.4

5. Determine the initial voltage across each component for the circuit shown in Figure 9.7.5 .

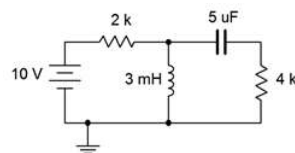


Figure 9.7.5

6. Given the network shown in Figure 9.7.5 , determine the steady-state voltage across each component.
7. Given the network shown in Figure 9.7.6 , determine the steady-state voltage across each component.

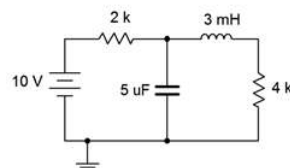


Figure 9.7.6

8. Determine the initial voltage across each component for the circuit shown in Figure 9.7.6 .

9. Given the network shown in Figure 9.7.7 , determine the steady-state voltage across each component.

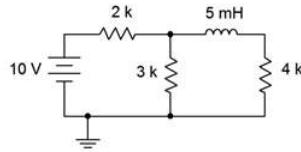


Figure 9.7.7

10. Determine the initial voltage across each component for the circuit shown in Figure 9.7.7 .

11. Determine the initial voltage across each component for the circuit shown in Figure 9.7.8 .

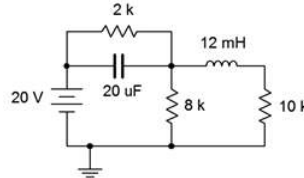


Figure 9.7.8

12. Given the network shown in Figure 9.7.8 , determine the steady-state voltage across each component.

13. Given the network shown in Figure 9.7.9 , determine the steady-state voltage across each component.

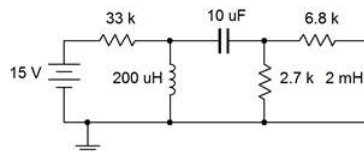


Figure 9.7.9

14. Determine the initial voltage across each component for the circuit shown in Figure 9.7.9 .

15. For the circuit shown in Figure 9.7.10 , determine the inductor current 20 microseconds after the power is switched on. Assume this is an ideal inductor with no internal resistance.

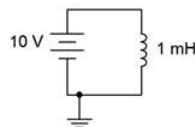


Figure 9.7.10

16. For the circuit shown in Figure 9.7.11 , determine the inductor current 100 milliseconds after the power is switched on. Assume this is an ideal inductor with no internal resistance.

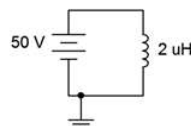


Figure 9.7.11

17. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 9.7.12 .

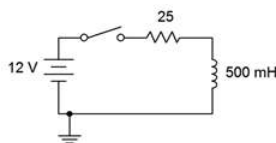


Figure 9.7.12

18. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 9.7.13 .

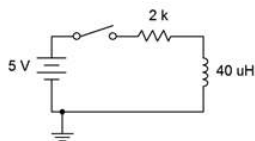


Figure 9.7.13

19. Given the circuit shown in Figure 9.7.2 , determine the inductor voltage and circulating current 200 milliseconds and 2 seconds after the switch is thrown. How does this change if we include $5\ \Omega$ of internal resistance to the inductor?

20. For the circuit shown in Figure 9.7.13 , determine the inductor voltage and circulating current 50 nanoseconds and 100 milliseconds after the switch is thrown.

21. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 9.7.14 , switch position 1.

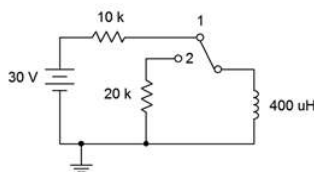


Figure 9.7.14

22. Determine the charge and discharge time constants for the circuit shown in Figure 9.7.15 .

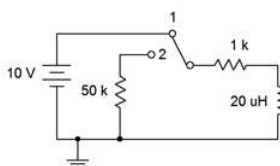


Figure 9.7.15

23. Given the circuit shown in Figure 9.7.14 , determine the inductor current 1 millisecond after the power is turned on. At this point, the switch is thrown to position 2. Determine the inductor voltage the instant of switch contact (assume ideal switch).

24. For the circuit shown in Figure 9.7.15 , determine the inductor current 400 microseconds after the power is turned on. At this point, the switch is thrown to position 2. Determine the inductor voltage the instant of switch contact (assume ideal switch).

25. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 9.7.16 , switch position 1.

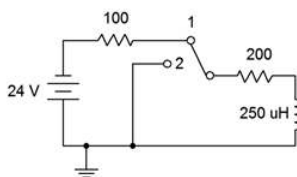


Figure 9.7.16

26. Given the circuit shown in Figure 9.7.16 , determine both the inductor current and voltage 10 milliseconds after the power is turned on. At this point, the switch is thrown to position 2. Determine how long it will take the inductor to discharge to nearly zero amps. Assume ideal switch.

Design

27. For Figure 9.7.12 , determine a new resistor value such that steady-state is reached in 2 milliseconds.

28. For Figure 9.7.13 , determine a new inductor value such that steady-state is reached in 5 microseconds.

Challenge

29. Determine the time constant and the time required to reach steady-state for the circuit shown in Figure 9.7.17 .

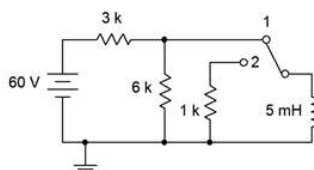


Figure 9.7.17

30. For the circuit shown in Figure 9.7.17 , determine the inductor voltage 400 microseconds after the power is turned on. At this point, the switch is thrown to position 2. Determine how long it will take the inductor to discharge to nearly zero amps. Assume ideal switch.

Simulation

31. Use a transient analysis to verify the time constant and time to steady-state of Figure 9.7.13 (problem 18).

32. Use a transient analysis to verify the inductor voltage waveform of Figure 9.7.12 as specified in problem 19.

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SECTION OVERVIEW

7.1: Introduction to RL and RC Circuits

Objective

In this exercise, the DC steady state response of simple RL and RC circuits is examined. The transient behavior of RC circuits is also tested.

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[7.1.5: Procedure](#)

[7.1.6: Data Tables](#)

[7.1.7: Questions](#)

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7.1.1: Theory Overview

The DC steady state response of RL and RC circuits are essential opposite of each other: that is, once steady state is reached, capacitors behave as open circuits while inductors behave as short circuits. In practicality, steady state is reached after five time constants. The time constant for an RC circuit is simply the effective capacitance times the effective resistance, $\tau = RC$. In the inductive case, the time constant is the effective inductance divided by the effective resistance, $\tau = L/R$.

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7.1.2: Equipment

(1) DC power supply

model: _____ srn: _____

(1) DMM

model: _____ srn: _____

(1) Stop watch

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7.1.3: Components

(1) 1 μF

actual: _____

(1) 470 μF

actual: _____

(1) 10 mH

actual: _____

(1) 10 $\text{k}\Omega$

actual: _____

(1) 47 $\text{k}\Omega$

actual: _____

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7.1.4: Schematics

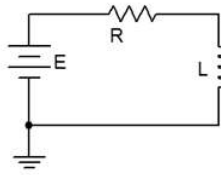


Figure 7.1.4.1

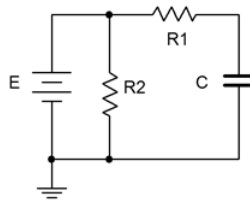


Figure 7.1.4.2

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7.1.5: Procedure

1.5.1: RL Circuit

1. Using Figure 1.4.1 with $E = 10\text{ V}$, $R = 47\text{ k}\Omega$, and $L = 10\text{ mH}$, calculate the time constant and record it in Table 1.6.1. Also, calculate and record the expected steady state inductor voltage in Table 1.6.2.
2. Set the power supply to 10 V but do not hook it up to the remainder of the circuit. After connecting the resistor and inductor, connect the DMM across the inductor set to read DC voltage (20 volt scale).
3. Connect the power supply to the circuit. The circuit should reach steady state very quickly, in much less than one second. Record the experimental inductor voltage in Table 1.6.2. Also, compute and record the percent deviation between experimental and theory in Table 1.6.2.

1.5.2: RC Circuit

4. Using Figure 1.4.2 with $E = 10\text{ V}$, $R_1 = 47\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$ and $C = 1\text{ }\mu\text{F}$, calculate the time constant and record it in Table 1.6.3. Also, calculate and record the expected steady state capacitor voltage in Table 1.6.4.
5. Set the power supply to 10 V but do not hook it up to the remainder of the circuit. After connecting the resistors and capacitor, connect the DMM across the capacitor set to read DC voltage (20 volt scale).
6. Connect the power supply to the circuit. The circuit should reach steady state quickly, in under one second. Record the experimental capacitor voltage in Table 1.6.4. Also, compute and record the percent deviation between experimental and theory in Table 1.6.4.

1.5.3: RC Circuit (long time constant)

7. Using Figure 1.4.2 with $E = 10\text{ V}$, $R_1 = 47\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$ and $C = 470\text{ }\mu\text{F}$, calculate the time constants and record them in Table 1.6.5. Also, calculate and record the expected steady state capacitor voltage (charge phase) in Table 1.6.5.
8. Set the power supply to standby, and after waiting a moment for the capacitor to discharge, remove the capacitor and replace it with the $470\text{ }\mu\text{F}$. Connect the DMM across the capacitor set to read DC voltage (20 volt scale).
9. Energize the circuit and record the capacitor voltage every 10 seconds as shown in Table 1.6.6. This is the charge phase.
10. Disconnect the power supply from the circuit and record the capacitor voltage every 10 seconds as shown in Table 1.6.7. This is the discharge phase.
11. Using the data from Tables 1.6.6 and 1.6.7, create two plots of capacitor voltage versus time and compare them to the theoretical plots found in the text.

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7.1.6: Data Tables

τ	
--------	--

Table 7.1.6.1

V_L Theory	V_L Experimental	Deviation

Table 7.1.6.2

τ	
--------	--

Table 7.1.6.3

V_C Theory	V_C Experimental	Deviation

Table 7.1.6.4

τ charge	
τ discharge	
V_C Theory	

Table 7.1.6.5

Time (sec)	Voltage
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	
110	
120	

Table 7.1.6.6

Time (sec)	Voltage
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	
110	
120	
130	
140	
150	

Table 7.1.6.7

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7.1.7: Questions

1. What is a reasonable approximation for an inductor at DC steady state?
 2. What is a reasonable approximation for a capacitor at DC steady state?
 3. How can a reasonable approximation for time-to-steady state of an RC circuit be computed?
 4. In general, what sorts of shapes do the charge and discharge voltages of DC RC circuits follow?
-

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SECTION OVERVIEW

7.2: Phasor Vector Review

Objective

The proper manipulation and representation of vectors is paramount for AC circuit analysis. Addition, subtraction, multiplication and division of vectors in both rectangular and polar forms are examined in both algebraic and graphical forms. Representations of waveforms using both phasor and time domain graphs are also examined.

7.2.1: Procedure

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7.2.1: Procedure

Perform the following operations, including phasor diagrams where appropriate.

1. $(6 + j10) + (8 - j2)$
2. $(2 + j5) - (10 - j4)$
3. $10 \angle 0^\circ + 20 \angle 90^\circ$
4. $10 \angle 45^\circ + 2 \angle -30^\circ$
5. $20 \angle 10^\circ - 5 \angle 75^\circ$
6. $(10 + j20) * (5 + j5)$
7. $(2 + j10) / (0.5 + j2)$
8. $10 \angle 0^\circ * 10 \angle 90^\circ$
9. $10 \angle 45^\circ * 10 \angle -45^\circ$
10. $10 \angle 90^\circ / 5 \angle 10^\circ$
11. $10 \angle 90^\circ / 40 \angle -40^\circ$
12. $1 / 200 \angle 90^\circ$

Draw the following expressions as time domain graphs.

13. $v = 10 \sin 2\pi 100t$
14. $v = 20 \sin 2\pi 1000t + 45^\circ$
15. $v = 5 + 6 \sin 2\pi 100t$

Write the expressions for the following descriptions.

16. A 10 volt peak sine wave at 20 Hz
17. A 5 peak to peak sine wave at 100 Hz with a -1 VDC offset
18. A 10 volt RMS sine wave at 1 kHz lagging by 40 degrees
19. A 20 volt peak sine wave at 10 kHz leading by 20 degrees with a 5 VDC offset

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SECTION OVERVIEW

7.3: The Oscilloscope (Tektronix MDO 3000 series)

Objective

This exercise is of a particularly practical nature, namely, introducing the use of the oscilloscope. The various input scaling, coupling, and triggering settings are examined along with a few specialty features.

7.3.1: Theory Overview

7.3.2: Equipment

7.3.3: Components

7.3.4: Schematics and Diagrams

7.3.5: Procedure

7.3.6: Data Tables

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7.3.1: Theory Overview

The oscilloscope (or simply scope, for short) is arguably the single most useful piece of test equipment in an electronics laboratory. The primary purpose of the oscilloscope is to plot a voltage versus time although it can also be used to plot one voltage versus another voltage, and in some cases, to plot voltage versus frequency. Oscilloscopes are capable of measuring both AC and DC waveforms, and unlike typical DMMs, can measure AC waveforms of very high frequency (typically 100 MHz or more versus an upper limit of around 1 kHz for a general purpose DMM). It is also worth noting that a DMM will measure the RMS value of an AC sinusoidal voltage, not its peak value.

While the modern digital oscilloscope on the surface appears much like its analog ancestors, the internal circuitry is far more complicated and the instrument affords much greater flexibility in measurement. Modern digital oscilloscopes typically include measurement aides such as horizontal and vertical cursors or bars, as well as direct readouts of characteristics such as waveform amplitude and frequency. At a minimum, modern oscilloscopes offer two input measurement channels although four and eight channel instruments are increasing in popularity.

Unlike handheld DMMs, most oscilloscopes measure voltages with respect to ground, that is, the inputs are not floating and thus the black, or ground, lead is always connected to the circuit ground or common node. This is an extremely important point as failure to remember this may lead to the inadvertent short circuiting of components during measurement. The standard accepted method of measuring a non-ground referenced potential is to use two probes, one tied to each node of interest, and then setting the oscilloscope to subtract the two channels rather than display each separately. Note that this technique is not required if the oscilloscope has floating inputs (for example, in a handheld oscilloscope). Further, while it is possible to measure non-ground referenced signals by floating the oscilloscope itself through defeating the ground pin on the power cord, this is a safety violation and should not be done.

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7.3.2: Equipment

(1) DC power supply

model: _____ srn: _____

(1) AC function generator

model: _____ srn: _____

(1) Digital multimeter

model: _____ srn: _____

(1) Oscilloscope, Tektronix MDO 3000 series

model: _____ srn: _____

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7.3.3: Components

(1) 10 k Ω

actual: _____

(1) 33 k Ω

actual: _____

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7.3.4: Schematics and Diagrams

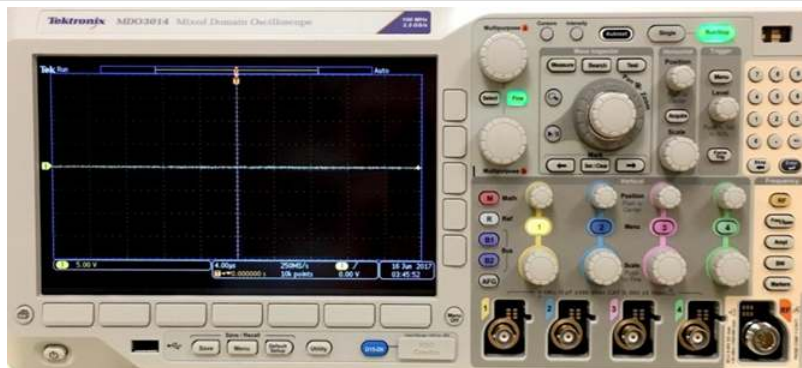


Figure 7.3.4.1

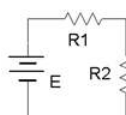


Figure 7.3.4.2

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7.3.5: Procedure

1. Figure 3.4.1 is a photo of the face of a Tektronix MDO 3000 series oscilloscope. Compare this to the bench oscilloscope and identify the following elements:

- Channel one through four BNC input connectors.
- RF input connector and settings section.
- Channel one through four select buttons.
- Horizontal Scale (i.e., Sensitivity) and Position knobs.
- Four Vertical Scale (i.e., Sensitivity) and Position knobs.
- Trigger Level knob.
- **Math** and **Measure** (in **Wave Inspector**) buttons.
- **Save** button (below display).
- **Autoset** button.
- **Menu Off** button.

2. Note the numerous buttons along the bottom and side of the display screen. These menu buttons are context-sensitive and their function will depend on the most recently selected button or knob. Menus may be removed from the display by pressing the **Menu Off** button (multiple times for nested menus). Power up the oscilloscope. Note that the main display is similar to a sheet of graph paper. Each square will have an appropriate scaling factor or weighting, for example, 1 volt per division vertically or 2 milliseconds per division horizontally. Waveform voltages and timings may be determined directly from the display by using these scales.

3. Select the channel one and two buttons (yellow and blue) and also press the **Autoset** button. (Autoset tries to create reasonable settings based on the input signal and is useful as a sort of “panic button”). There should now be two horizontal lines on the display, one yellow and one blue. These traces may be moved vertically on the display via the associated Position knobs. Also, a trace can be removed by deselecting the corresponding channel button. The Vertical and Horizontal Scale knobs behave in a similar fashion and do not include calibration markings. That is because the settings for these knobs show up on the main display. Adjust the Scale knobs and note how the corresponding values at the bottom of the display change. Voltages are in a 1/2/5 scale sequence while Time is in a 1/2/4 scale sequence.

4. When an input is selected, a menu will pop up allowing control over that input's basic settings. One of the more important fundamental settings on an oscilloscope channel is the **Input Coupling**. This is controlled via one of the bottom row buttons. There are two choices: **AC** allows only AC signals through thus blocking DC, and **DC** allows all signals through (it does not prevent AC).

5. Set the channel one Vertical Scale to 5 volts per division. Set the channel two Scale to 2 volts per division. Set the Time (Horizontal) Scale to 1 millisecond per division. Finally, set the input Coupling to DC for both input channels and align the blue and yellow display lines to the center line of the display via the Vertical Position knob (note that pushing the vertical Position knobs will automatically center the trace).

6. Build the circuit of Figure 3.4.2 using $E = 10\text{ V}$, $R_1 = 10\text{ k}\Omega$ and $R_2 = 33\text{ k}\Omega$. Connect a probe from the channel one input to the power supply (red or tip to the positive terminal, black clip to ground). Connect a second probe from channel two to R_2 (again, red or tip to the high side of the resistor and the black clip to ground).

7. The yellow and blue lines should have deflected upward. Channel one should be raised two divisions (2 divisions at 5 volts per division yields the 10 volt source). Using this method, determine the voltage across R_2 (remember, input two should have been set for 2 volts per division). Calculate the expected voltage across R_2 using measured resistor values and compare the two in Table 3.6.1. Note that it is not possible to achieve extremely high precision using this method (e.g., four or more digits). Indeed, a DMM is often more useful for direct measurement of DC potentials. Double check the results using a DMM and the final column of Table 3.6.1.

8. Select AC Coupling for the two inputs. The flat DC lines should drop back to zero. This is because AC Coupling blocks DC. This will be useful for measuring the AC component of a combined AC/DC signal, such as might be seen in an audio amplifier. Set the input coupling for both channels back to DC.

9. Replace the DC power supply with the function generator. Set the function generator for a one volt peak sine wave at 1 kHz and apply it to the resistor network. The display should now show two small sine waves. Adjust the Vertical Scale settings for the two inputs so that the waves take up the majority of the display. If the display is very blurry with the sine waves appearing to jump about side to side, the Trigger Level may need to be adjusted. Also, adjust the Time Scale so that only one or two cycles of the wave may be seen. Using the Scale settings, determine the two voltages (following the method of step 7) as well as the waveform's period and compare them to the values expected via theory, recording the results in Tables 3.6.2 and 3.6.3. Also crosscheck the results using a DMM to measure the RMS voltages.

10. To find the voltage across R1, the channel two voltage (V_{R2}) may be subtracted from channel one (E source) via the **Math** function. Use the red button to select the **Math** function and create the appropriate expression from the menu ($ch1 - ch2$). This display shows up in red. To remove a waveform, press its button again. Remove the math waveform before proceeding to the next step.

11. One of the more useful aspects of the oscilloscope is the ability to show the actual waveshape. This may be used, for example, as a means of determining distortion in an amplifier. Change the waveshape on the function generator to a square wave, triangle, or other shape and note how the oscilloscope responds. Note that the oscilloscope will also show a DC component, if any, as the AC signal being offset or "riding on the DC". Adjust the function generator to add a DC offset to the signal and note how the oscilloscope display shifts. Return the function generator back to a sine wave and remove any DC offset.

12. It is often useful to take precise differential measurement on a waveform. For this, the bars or cursors are useful. Select the **Cursors** button toward the top of the oscilloscope. From the menu on the display, select **Vertical Bars**. Two vertical bars will appear on the display (it is possible that one or both could be positioned off the main display). They may be moved left and right via the Multipurpose knobs (next to the Cursors button). The **Select** button toggles between independent and tandem cursor movement. A read out of the bar values will appear in the upper portion of the display. They indicate the positions of the cursors, i.e., the location where they cross the waveform. Vertical Bars are very useful for obtaining time information as well as amplitudes at specific points along the wave. A similar function is the Horizontal Bars which are particularly useful for determining amplitudes. Try the Horizontal Bars by selecting them via the Cursors menu again (holding the **Cursors** button will bring up the menu).

13. For some waveform parameters, automatic readings are available. These are accessed via the **Measure** button. Press **Measure**, select **Add Measurement**, and page through the various options using the Multipurpose knob. Select **Frequency**. Note that a small readout of the frequency will now appear on the display. Multiple measurements are possible simultaneously. Important: There are specific limits on the proper usage of these measurements. If the guidelines are not followed, erroneous values may result. Always perform an approximation via the Scale factor and divisions method even when using an automatic measurement!

14. Finally, a snap-shot of the screen may be saved for future work using the USB port and a USB memory stick via the **Save Menu** button. The pop up menu has options for saving the image as well as the trace data or setup info. **Select Save Screen Image** to save a bit mapped graphics file that can be used as is or processed further in a graphics program (for example, inverting the colors for printing). The .PNG format is recommended.

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7.3.6: Data Tables

V_{R2}	Scale (V/Div)	Number of Divisions	Voltage Scope	Voltage DMM
Oscilloscope				
Theory	X	X		

Table 7.3.6.1

	Scale (V/Div)	Number of Divisions	Voltage Peak	Voltage RMS
E Oscilloscope				
E Theory	X	X		
V_{R2} Oscilloscope				
V_{R2} Theory	X	X		

Table 7.3.6.2

	Scale (S/Div)	Number of Divisions	Period	Frequency
E Oscilloscope				
E Theory	X	X		

Table 7.3.6.3

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CHAPTER OVERVIEW

8: Introduction to RL and RC Circuits

Objective

In this exercise, the DC steady state response of simple RL and RC circuits is examined. The transient behavior of RC circuits is also tested.

[8.1: Theory Overview](#)

[8.2: Equipment](#)

[8.3: Components](#)

[8.4: Schematics](#)

[8.5: Procedure](#)

[8.6: Data Tables](#)

[8.7: Questions](#)

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8.1: Theory Overview

The DC steady state response of RL and RC circuits are essential opposite of each other: that is, once steady state is reached, capacitors behave as open circuits while inductors behave as short circuits. In practicality, steady state is reached after five time constants. The time constant for an RC circuit is simply the effective capacitance times the effective resistance, $\tau = RC$. In the inductive case, the time constant is the effective inductance divided by the effective resistance, $\tau = L/R$.

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8.2: Equipment

(1) DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(1) Stop watch

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8.3: Components

(1) $1\ \mu\text{F}$

actual: _____

(1) $470\ \mu\text{F}$

actual: _____

(1) $10\ \text{mH}$

actual: _____

(1) $10\ \text{k}\Omega$

actual: _____

(1) $47\ \text{k}\Omega$

actual: _____

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8.4: Schematics

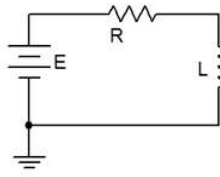


Figure 8.4.1

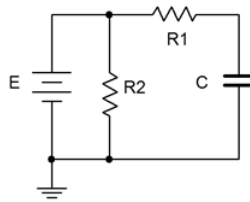


Figure 8.4.2

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8.5: Procedure

1.5.1: RL Circuit

1. Using Figure 1.4.1 with $E = 10\text{ V}$, $R = 47\text{ k}\Omega$, and $L = 10\text{ mH}$, calculate the time constant and record it in Table 1.6.1. Also, calculate and record the expected steady state inductor voltage in Table 1.6.2.
2. Set the power supply to 10 V but do not hook it up to the remainder of the circuit. After connecting the resistor and inductor, connect the DMM across the inductor set to read DC voltage (20 volt scale).
3. Connect the power supply to the circuit. The circuit should reach steady state very quickly, in much less than one second. Record the experimental inductor voltage in Table 1.6.2. Also, compute and record the percent deviation between experimental and theory in Table 1.6.2.

1.5.2: RC Circuit

4. Using Figure 1.4.2 with $E = 10\text{ V}$, $R_1 = 47\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$ and $C = 1\text{ }\mu\text{F}$, calculate the time constant and record it in Table 1.6.3. Also, calculate and record the expected steady state capacitor voltage in Table 1.6.4.
5. Set the power supply to 10 V but do not hook it up to the remainder of the circuit. After connecting the resistors and capacitor, connect the DMM across the capacitor set to read DC voltage (20 volt scale).
6. Connect the power supply to the circuit. The circuit should reach steady state quickly, in under one second. Record the experimental capacitor voltage in Table 1.6.4. Also, compute and record the percent deviation between experimental and theory in Table 1.6.4.

1.5.3: RC Circuit (long time constant)

7. Using Figure 1.4.2 with $E = 10\text{ V}$, $R_1 = 47\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$ and $C = 470\text{ }\mu\text{F}$, calculate the time constants and record them in Table 1.6.5. Also, calculate and record the expected steady state capacitor voltage (charge phase) in Table 1.6.5.
8. Set the power supply to standby, and after waiting a moment for the capacitor to discharge, remove the capacitor and replace it with the $470\text{ }\mu\text{F}$. Connect the DMM across the capacitor set to read DC voltage (20 volt scale).
9. Energize the circuit and record the capacitor voltage every 10 seconds as shown in Table 1.6.6. This is the charge phase.
10. Disconnect the power supply from the circuit and record the capacitor voltage every 10 seconds as shown in Table 1.6.7. This is the discharge phase.
11. Using the data from Tables 1.6.6 and 1.6.7, create two plots of capacitor voltage versus time and compare them to the theoretical plots found in the text.

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8.6: Data Tables

τ	
--------	--

Table 8.6.1

V_L Theory	V_L Experimental	Deviation

Table 8.6.2

τ	
--------	--

Table 8.6.3

V_C Theory	V_C Experimental	Deviation

Table 8.6.4

τ charge	
τ discharge	
V_C Theory	

Table 8.6.5

Time (sec)	Voltage
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	
110	
120	

Table 8.6.6

Time (sec)	Voltage
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	
110	
120	
130	
140	
150	

Table 8.6.7

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8.7: Questions

1. What is a reasonable approximation for an inductor at DC steady state?
 2. What is a reasonable approximation for a capacitor at DC steady state?
 3. How can a reasonable approximation for time-to-steady state of an RC circuit be computed?
 4. In general, what sorts of shapes do the charge and discharge voltages of DC RC circuits follow?
-

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CHAPTER OVERVIEW

9: Series RLC Circuits

Objective

This exercise examines the voltage and current relationships in series R, L, C networks. Of particular importance is the phase of the various components and how Kirchhoff's voltage law is extended for AC circuits. Both time domain and phasor plots of the voltages are generated.

[9.1: Theory Overview](#)

[9.2: Equipment](#)

[9.3: Components](#)

[9.4: Schematics](#)

[9.5: Procedure](#)

[9.6: Data Tables](#)

[9.7: Questions](#)

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9.1: Theory Overview

Each element has a unique phase response: for resistors, the voltage is always in phase with the current, for capacitors the voltage always lags the current by 90 degrees, and for inductors the voltage always leads the current by 90 degrees. Consequently, a series combination of R, L, and C components will yield a complex impedance with a phase angle between +90 and -90 degrees. Due to the phase response, Kirchhoff's voltage law must be computed using vector (phasor) sums rather than simply relying on the magnitudes. Indeed, all computations of this nature, such as a voltage divider, must be computed using vectors.

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9.2: Equipment

(1) AC function generator

model: _____ srn: _____

(1) Oscilloscope

model: _____ srn: _____

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9.3: Components

(1) 10 nF

actual: _____

(1) 10 mH

actual: _____

(1) 1 k Ω

actual: _____

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9.4: Schematics

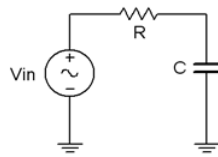


Figure 9.4.1

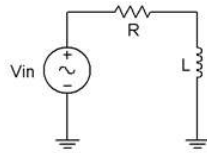


Figure 9.4.2

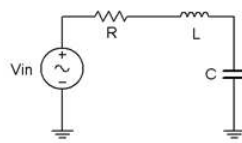


Figure 9.4.3

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9.5: Procedure

8.5.1: RC Circuit

1. Using Figure 8.4.1 with $V_{in} = 2\text{ V}$ p-p sine at 10 kHz, $R = 1\text{ k}\Omega$, and $C = 10\text{ nF}$, determine the theoretical capacitive reactance and circuit impedance, and record the results in Table 8.6.1 (the experimental portion of this table will be filled out in step 5). Using the voltage divider rule, compute the resistor and capacitor voltages and record them in Table 8.6.2.
2. Build the circuit of Figure 8.4.1 using $R = 1\text{ k}\Omega$, and $C = 10\text{ nF}$. Place one probe across the generator and another across the capacitor. Set the generator to a 10 kHz sine wave and 2 V p-p. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings. Also, consider using Averaging for the acquisition mode, particularly to clean up signals derived using the Math function.
3. Measure the peak-to-peak voltage across the capacitor and record in Table 8.6.2. Along with the magnitude, be sure to record the time deviation between V_C and the input signal (from which the phase may be determined). Using the Math function, measure and record the voltage and time delay for the resistor ($V_{in}-V_C$). Compute the phase angle and record these values in Table 8.6.2.
4. Take a snapshot of the oscilloscope displaying V_{in} , V_C , and V_R .
5. Compute the deviations between the theoretical and experimental values of Table 8.6.2 and record the results in the final columns of Table 8.6.2. Based on the experimental values, determine the experimental Z and X_C values via Ohm's law ($i = V_R/R$, $X_C = V_C/i$, $Z = V_{in}/i$) and record back in Table 8.6.1 along with the deviations.
6. Create a phasor plot showing V_{in} , V_C , and V_R . Include both the time domain display from step 4 and the phasor plot with the technical report.

8.5.2: RL Circuit

7. Replace the capacitor with the 10 mH inductor (i.e. Figure 8.4.2), and repeat steps 1 through 6 in like manner, using Tables 8.6.3 and 8.6.4.

8.5.3: RLC Circuit

8. Using Figure 8.4.3 with both the 10 nF capacitor and 10 mH inductor, repeat steps 1 through 6 in similar manner, using Tables 8.6.5 and 8.6.6. Using a four channel oscilloscope: To obtain proper readings, place the first probe at the input, the second probe between the resistor and inductor, and the third probe between the inductor and capacitor. Probe three yields V_C . Using the Math function, probe two minus probe three yields V_L , and finally, probe one minus probe two yields V_R . Assigning Reference waveforms can be useful to see all of the signals together. Using a two channel oscilloscope: Unfortunately, it will be impossible to see the voltage of all three components simultaneously with the source voltage using a two channel oscilloscope. To obtain proper readings, place the first probe at the input and the second probe across the capacitor in order to see the phase and magnitude of V_C . Then, swap C and L (placing the second probe across the inductor) to see V_L , and finally, swap L and R (with the second probe across R) in order see V_R .

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9.6: Data Tables

8.6.1: RC Circuit

	Theory	Experimental	% Deviation
X_C			
Z Magnitude			
Z θ			

Table 9.6.1

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
V_C							
V_R							

Table 9.6.2

8.6.2: RL Circuit

	Theory	Experimental	% Deviation
X_L			
Z Magnitude			
Z θ			

Table 9.6.3

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
V_L							
V_R							

Table 9.6.4

8.6.3: RLC Circuit

	Theory	Experimental	% Deviation
X_C			
X_L			
Z Magnitude			
Z θ			

Table 9.6.5

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
V_C							
V_L							
V_R							

Table 9.6.6

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9.7: Questions

1. What is the phase relationship between R, L, and C components in a series AC circuit?
 2. Based on measurements, does Kirchhoff's voltage law apply to the three tested circuits (show work)?
 3. In general, how would the phasor diagram of Figure 8.6.1 change if the frequency was raised?
 4. In general, how would the phasor diagram of Figure 8.6.2 change if the frequency was lowered?
-

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CHAPTER OVERVIEW

10: Parallel RLC Circuits

Objective

This exercise examines the voltage and current relationships in parallel R, L, C networks. Of particular importance is the phase of the various components and how Kirchhoff's current law is extended for AC circuits. Both time domain and phasor plots of the currents are generated. A technique to measure current using a current sense resistor will also be explored.

[10.1: Theory Overview](#)

[10.2: Equipment](#)

[10.3: Components](#)

[10.4: Schematics](#)

[10.5: Procedure](#)

[10.6: Data Tables](#)

[10.7: Questions](#)

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10.1: Theory Overview

Recall that for resistors, the voltage is always in phase with the current, for capacitors the voltage always lags the current by 90 degrees, and for inductors the voltage always leads the current by 90 degrees. Because each element has a unique phase response between +90 and -90 degrees, a parallel combination of R, L, and C components will yield a complex impedance with a phase angle between +90 and -90 degrees. Due to the phase response, Kirchhoff's current law must be computed using vector (phasor) sums rather than simply relying on the magnitudes. Indeed, all computations of this nature, such as a current divider, must be computed using vectors.

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10.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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10.3: Components

(1) 10 nF

actual: _____

(1) 10 mH

actual: _____

(1) 1 k Ω

actual: _____

(3) 10 Ω

actual: _____

actual: _____

actual: _____

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10.4: Schematics

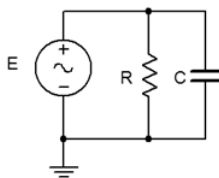


Figure 10.4.1

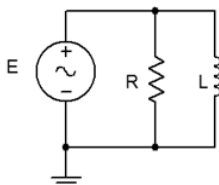


Figure 10.4.2

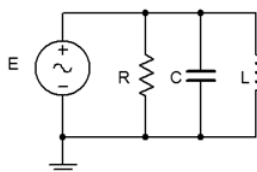


Figure 10.4.3

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10.5: Procedure

9.5.1: RC Circuit

1. Using Figure 9.4.1 with a 10 V p-p 10 kHz source, $R = 1\text{ k}\Omega$, and $C = 10\text{ nF}$, determine the theoretical capacitive reactance and circuit impedance, and record the results in Table 9.6.1 (the experimental portion of this table will be filled out in step 6). Using the current divider rule, compute the resistor and capacitor currents and record them in Table 9.6.2.
2. Build the circuit of Figure 9.4.1 using $R = 1\text{ k}\Omega$, and $C = 10\text{ nF}$. A common method to measure current using the oscilloscope is to place a small current sense resistor in line with the current of interest. If the resistor is much smaller than the surrounding reactances it will have a minimal effect on the current. Because the voltage and current of the resistor are always in phase with each other, the relative phase of the current in question must be the same as that of the sensing resistor's voltage. Each of the three circuit currents will be measured separately and with respect to the source in order to determine relative phase. To measure the total current, place a $10\text{ }\Omega$ resistor between ground and the bottom connection of the parallel components. Set the generator to a 10 V p-p sine wave at 10 kHz. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings. Also, consider using waveform averaging, particularly to clean up signals derived via the Math function.
3. Place probe one across the generator and probe two across the sense resistor. Measure the voltage across the sense resistor, calculate the corresponding total current via Ohm's law and record in Table 9.6.2. Along with the magnitude, be sure to record the time deviation between the sense waveform and the input signal (from which the phase may be determined eventually).
4. Remove the main sense resistor and place one $10\text{ }\Omega$ resistor between the capacitor and ground to serve as the capacitor current sense. Place a second $10\text{ }\Omega$ resistor between the resistor and ground to sense the resistor current. Leave probe one at the generator and move probe two across the sense resistor in the resistor branch. Repeat the Ohm's law process to obtain its current, recording the magnitude and phase angle in Table 9.6.2. Finally, move probe two so that it is across the capacitor's sense resistor. Measure and record the appropriate values in Table 9.6.2. Note that if you are using a four channel oscilloscope, simultaneous input, resistor and capacitor measurements are possible.
5. Move probe one to the resistor's sense resistor and leave probe two at the capacitor's sense resistor. Save a picture of the oscilloscope displaying the voltage waveforms representing i_R , i_C and i_{in} (i.e., the Math waveform computed from $i_R + i_C$).
6. Compute the deviations between the theoretical and experimental values of Table 9.6.2 and record the results in the final columns of Table 9.6.2. Based on the experimental values, determine the experimental Z and X_C values via Ohm's law ($X_C = V_C/i_C$, $Z = V_{in}/i_{in}$) and record back in Table 9.6.1 along with the deviations.
7. Create a phasor plot showing i_{in} , i_C , and i_R . Include both the time domain display from step 4 and the phasor plot with the technical report.

9.5.2: RL Circuit

8. Replace the capacitor with the 10 mH inductor (i.e. Figure 9.4.2), and repeat steps 1 through 7 in like manner, using Tables 9.6.3 and 9.6.4.

9.5.3: RLC Circuit

9. Using Figure 9.4.3 with both the 10 nF capacitor and 10 mH inductor (and a third sense resistor), repeat steps 1 through 7 in like manner, using Tables 9.6.5 and 9.6.6. Note that it will not be possible to see all four waveforms simultaneously in step 5 if a two channel oscilloscope is being used. For a four channel oscilloscope, place a probe across each of the three sense resistors.

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10.6: Data Tables

9.6.1: RC Circuit

	Theory	Experimental	% Deviation
X_C			
Z Magnitude			
Z θ			

Table 10.6.1

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
i_C							
i_R							
i_{in}							

Table 10.6.2

9.6.2: RL Circuit

	Theory	Experimental	% Deviation
X_L			
Z Magnitude			
Z θ			

Table 10.6.3

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
i_L							
i_R							
i_{in}							

Table 10.6.4

9.6.3: RLC Circuit

	Theory	Experimental	% Deviation
X_C			
X_L			
Z Magnitude			
Z θ			

Table 10.6.5

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
i_C							
i_L							
i_R							
i_{in}							

Table 10.6.6

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10.7: Questions

1. What is the phase relationship between R, L, and C components in a parallel AC circuit?
 2. Based on measurements, does Kirchhoff's current law apply to the three tested circuits (show work)?
 3. In general, how would the phasor diagram of Figure 9.6.1 change if the frequency was raised?
 4. In general, how would the phasor diagram of Figure 9.6.2 change if the frequency was lowered?
-

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CHAPTER OVERVIEW

11: DC Operational Amplifiers (Op Amps)

11.1: Decibels and Bode Plots

11.1.1: Theory Overview

11.1.2: Reference

11.1.3: Equipment

11.1.4: Components

11.1.5: Schematics

11.1.6: Procedure

11.1.7: Data Tables

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11.2: The Differential Amplifier

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11.2.8: Questions

11.3: The Non-inverting Voltage Amplifier

11.3.1: Theory Overview

11.3.2: Reference

11.3.3: Equipment

11.3.4: Components

11.3.5: Schematics

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11.4: The Inverting Voltage Amplifier

11.4.1: Theory Overview

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11.4.4: Components

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11.4.7: Data Tables

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11.5: The Op Amp Differential Amplifier

11.5.1: Theory Overview

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- [11.5.4: Components](#)
- [11.5.5: Schematics](#)
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SECTION OVERVIEW

11.1: Decibels and Bode Plots

Objective

In this exercise, the usage of decibel measurements and Bode plots will be examined. The investigation will include the relationship between ordinary and decibel gain, and the decibel-amplitude and phase response of a simple lag network.

[11.1.1: Theory Overview](#)

[11.1.2: Reference](#)

[11.1.3: Equipment](#)

[11.1.4: Components](#)

[11.1.5: Schematics](#)

[11.1.6: Procedure](#)

[11.1.7: Data Tables](#)

[11.1.8: Questions](#)

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11.1.1.1: Theory Overview

The decibel is a logarithmic-based measurement scheme. It is based on ratios of change. Positive values indicate an increase while negative values indicate a decrease. Decibel schemes can be used for gains and, with minor modification, signal levels. A Bode plot shows the variations of gain (typically expressed in decibels) and phase across a range of frequencies for some particular circuit. These will prove to be very valuable in later design and analysis work.

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11.1.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 1.2, The Decibel

Section 1.3, Bode Plots

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11.1.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Decibel-reading voltmeter

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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11.1.4: Components

(1) 100n F

actual: _____

(1) 100 Ω

actual: _____

(1) 1k Ω

actual: _____

(1) 4k7 Ω

actual: _____

(2) 10k Ω

actual: _____

(1) 22k Ω

actual: _____

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11.1.5: Schematics

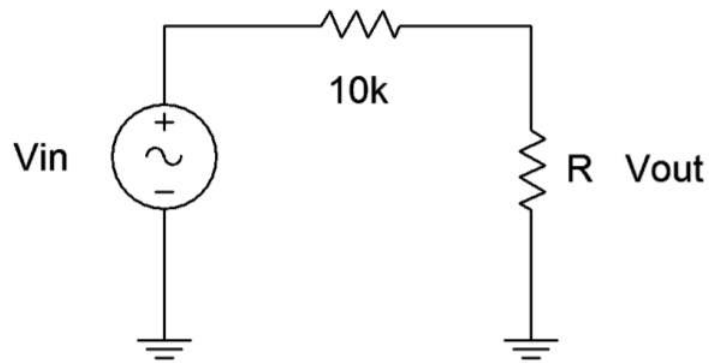


Figure 11.1.5.1

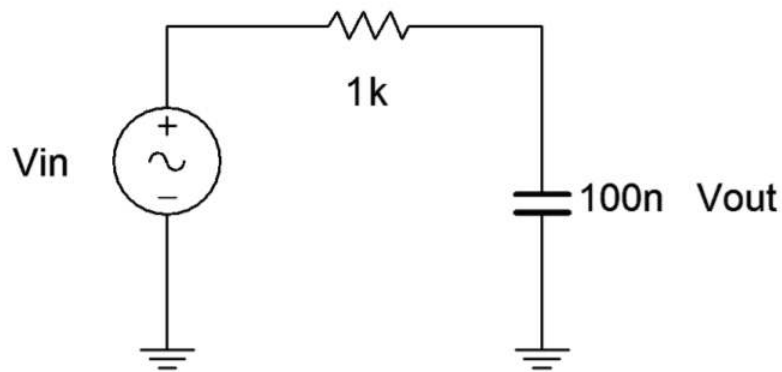


Figure 11.1.5.2

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11.1.6: Procedure

1. Calculate the voltage gains (losses) for the voltage divider of Figure 1.5.1 for the resistor values specified, and record them in Table 1.7.1. Also, convert each of the ordinary gains into decibel form.
2. Assemble the circuit of Figure 1.5.1 using the 22k resistor.
3. Set the generator to a 100 Hz sine wave, 0 dBV (Note: If the meter is calibrated in dBu, then use 0 dBu).
4. Apply the generator to the circuit. Measure and record the output voltage in Table 1.7.1 using the decibel-reading voltmeter. Also, compute the resulting experimental decibel voltage gain and gain deviation.
5. Repeat step 4 for the remaining resistor values in Table 1.7.1.
6. To create a simple Bode plot, the lag network of Figure 1.5.2 will be used. Assemble this circuit and record its theoretical critical frequency in Table 1.7.2.
7. Set the generator to a 1 kHz sine wave, 0 dBV.
8. Apply the generator to the circuit. Determine the experimental critical frequency by adjusting the frequency of the generator until the circuit's output voltage is -3 dBV. Record the measured frequency in Table 1.7.2.
9. Set the generator to a sine wave at one-tenth of the experimental critical frequency.
10. Adjust the generator's output level to 0 dBV.
11. Apply the generator to the circuit. Measure and record the output level in decibels in Table 1.7.3. Also, measure and record the phase angle between the input and output waveforms and record it in Table 1.7.3.
12. Repeat steps 9 through 11 for the remaining frequencies listed in Table 1.7.3.
13. Using the values from Table 1.7.3, create a Bode plot for this circuit using a log scaled horizontal axis (i.e., semi-log paper).

1.6.1: Computer Simulation

14. Build the lag network of Figure 1.5.2 in a simulator and run an AC Analysis. Be sure to run this from at least one decade below the critical frequency to at least one decade above. Also, use a decibel scale for the gain amplitude. Compare the results to the Bode plot generated in Step 13 and include this graph with the technical report.

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11.1.7: Data Tables

R	A_v Theory	A_v' Theory	V_{out}'	Experimental A_v'	% Deviation
22k Ω					
10k Ω					
4k7 Ω					
1k Ω					
100 Ω					

Table 11.1.7.1

Theoretical f_c	
Experimental f_c	

Table 11.1.7.2

Factor	Frequency	A_v'	Phase
.1 f_c			
.2 f_c			
.5 f_c			
f_c			
2 f_c			
5 f_c			
10 f_c			

Table 11.1.7.3

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11.1.8: Questions

1. Is the logarithmic nature of the decibel apparent in the data of Table 1.7.1?
 2. Using the plot created in step 13, determine the slope in dB-per-octave in the region above f_c .
 3. What would the plot of step 13 look like if ordinary gains had been used instead of decibel gains?
-

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SECTION OVERVIEW

11.2: The Differential Amplifier

Objective

In this exercise, the performance of a differential amplifier will be examined. The investigation will include the DC parameters of input bias and offset current, and output offset voltage. The AC parameters of interest are the differential and common-mode gains, and the resulting common-mode rejection-ratio (CMRR).

[11.2.1: Theory Overview](#)

[11.2.2: Reference](#)

[11.2.3: Equipment](#)

[11.2.4: Components](#)

[11.2.5: Schematics](#)

[11.2.6: Procedure](#)

[11.2.7: Data Tables](#)

[11.2.8: Questions](#)

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11.2.1: Theory Overview

The ideal differential amplifier is perfectly symmetrical producing identical DC input bias currents and output collector voltages. Several factors ranging from the mismatch of transistor parameters to resistor tolerances prevent perfect symmetry in a practical circuit. The DC quality of the circuit can be expressed in terms of the mismatches. The difference between the input bias currents is known as the input offset current. The difference between the output collector voltages is known as the output offset voltage. For AC performance, the primary items of concern are the differential and common-mode gains. The ideal differential amplifier will only amplify differential input signals, and thus, has a common-mode gain of zero. Due to component mismatches and internal design limits, the common-mode gain is never zero, allowing some portion of the common-mode input signal to make its way to the output. The measure of the suppression of common-mode signals is given by the common-mode rejection-ratio, or CMRR. CMRR can be found by dividing the differential gain by the common-mode gain.

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11.2.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 1.6, The Differential Amplifier

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11.2.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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11.2.4: Components

(3) Small signal NPN transistors (2N3904, 2N2222, etc.)

(2) 100 Ω

actual: _____

(2) 330 Ω

actual: _____

(2) 470 Ω

actual: _____

(1) 3k3 Ω

actual: _____

(2) 4k7 Ω

actual: _____

(1) 5k6 Ω

actual: _____

(1) 10k Ω

actual: _____

(2) 22k Ω

actual: _____

(1) 33k Ω

actual: _____

2N3904 Datasheet: <https://www.onsemi.com/pub/Collateral/2N3903-D.PDF>

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11.2.5: Schematics

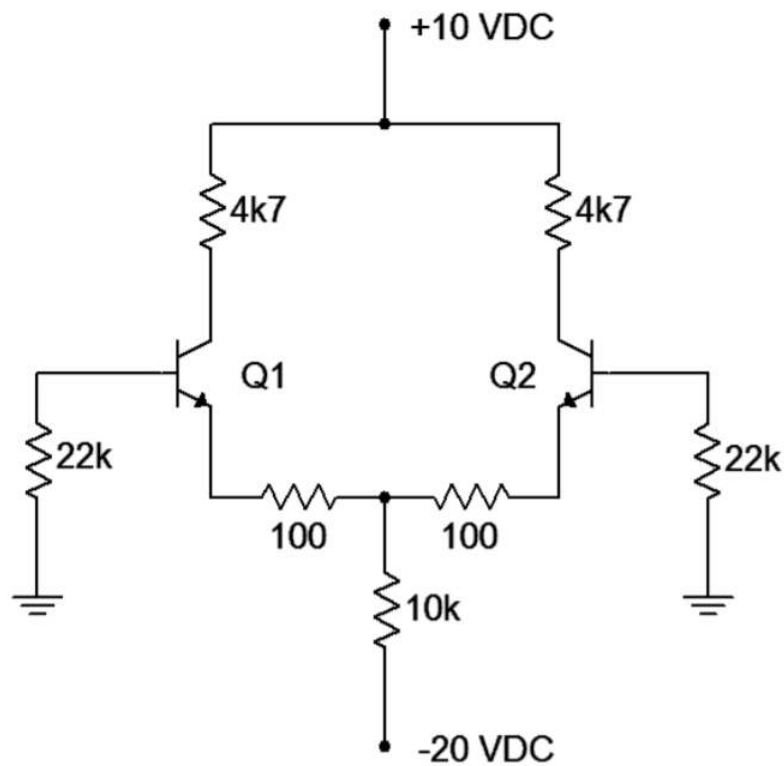


Figure 11.2.5.1

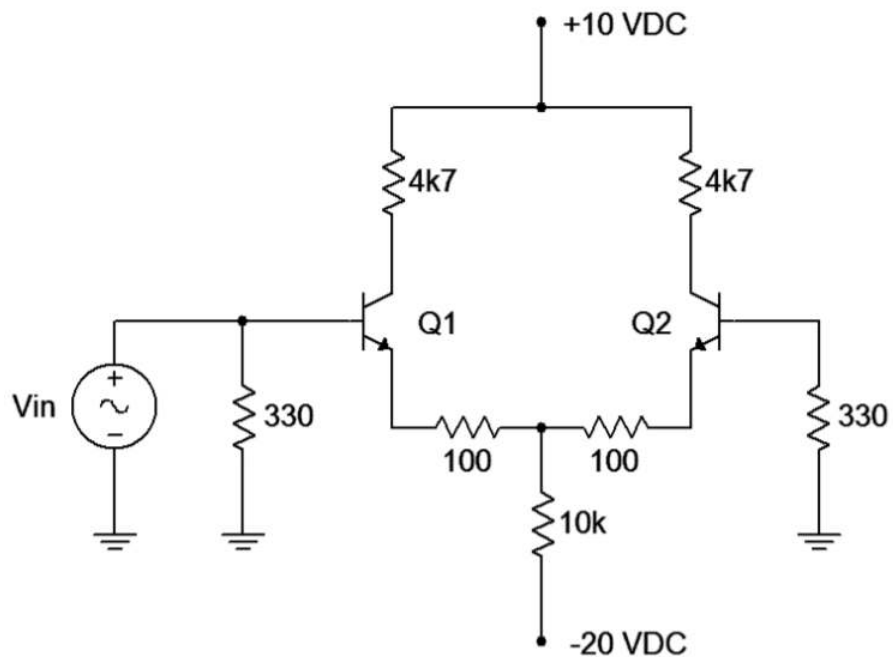


Figure 11.2.5.2

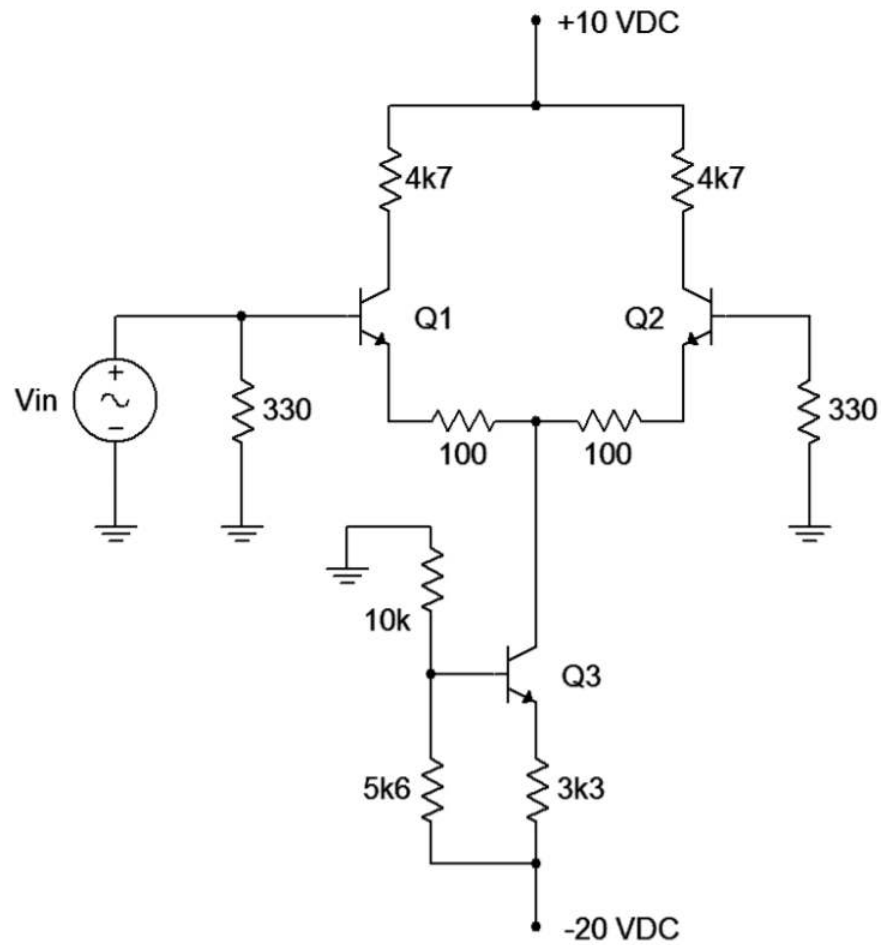


Figure 11.2.5.3

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11.2.6: Procedure

2.6.1: DC Parameters

1. Assume that the transistors of Figure 2.5.1 have a current gain of 150. Calculate the base currents and collector voltages for the amplifier of Figure 2.5.1 and record them in Table 2.7.1. Also, compute and record the theoretical (ideal) input offset current and output offset voltage.
2. Assemble the circuit of Figure 2.5.1.
3. Measure and record the base currents in Table 2.7.1. (Note: You may wish to measure the voltage across the base resistors and compute the base currents if the DMM cannot measure small DC currents.) Based on these currents, compute and record the experimental input bias and offset currents along with the corresponding deviations.
4. Measure and record the collector voltages in Table 2.7.1. Based on these voltages, compute and record the experimental output offset voltage and the corresponding deviation.

2.6.2: AC Parameters

5. Calculate the differential voltage gain and collector voltages for the amplifier of Figure 2.5.2 using an input of 20 millivolts, and record them in Table 2.7.2.
6. Assemble the circuit of Figure 2.5.2.
7. Set the generator to a 1 kHz sine wave, 20 millivolts peak.
8. Apply the generator to the amplifier. Measure and record the AC collector voltages in Table 2.7.2 while noting the phase relative to the input. Also, compute the resulting experimental voltage gain from the input to collector one, and the deviations.
9. Apply the generator to both inputs. Set the generator's output to 1 volt peak.
10. Measure the AC voltage at collector one and record it in Table 2.7.3.
11. Based on the value measured in step 10, compute and record the common-mode gain and CMRR in Table 2.7.3.

2.6.3: Improved CMRR

12. Assemble the circuit of Figure 2.5.3. This circuit uses an improved tail current source that exhibits much higher internal impedance than the circuit of Figure 2.5.2. This should yield a decrease in common mode gain which, in turn, should yield an improved CMRR. Note that the new circuit sets up virtually the same tail current, therefore producing approximately the same DC parameters and differential gain as the original.
13. Repeat steps 9 through 11 recording the results in Table 2.7.4.

2.6.4: Troubleshooting

14. Continuing with the amplifier of Figure 2.5.3, turn the signal down to 0. Estimate and then measure the results for each individual error presented in Table 2.7.5.

2.6.5: Computer Simulation

15. Build the amplifier of Figure 2.5.2 in a simulator and run a Transient Analysis echoing steps 5 through 8. Compare the results to the data found in Table 2.7.2.

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11.2.7: Data Tables

DC Quantity	Theoretical	Experimental	% Deviation
I_{B1}			
I_{B2}			
$I_{in-bias}$			
$I_{in-offset}$			n/a
V_{C1}			
V_{C2}			
$V_{out-offset}$			n/a

Table 11.2.7.1

AC Quantity	Theoretical	Experimental	% Deviation
V_{C1}			
V_{C2}			
A_v			

Table 11.2.7.2

V_{C1}	
A_{cm}	
CMRR	

Table 11.2.7.3

V_{C1}	
A_{cm}	
CMRR	

Table 11.2.7.4

Error	Quantity	Estimate	Actual
3k3 is replaced with 33k	V_{C1} DC		
Q_1 's 4k7 is 470	V_{C1} DC		
Both 4k7 are 470	V_{C1} DC		

Table 11.2.7.5

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11.2.8: Questions

1. How might the input offset current of Figure 2.5.1 be reduced?
 2. What are some causes of output offset voltage in the circuit of Figure 2.5.1?
 3. What are the effects if the two collector resistors not identical in value?
 4. What is the significance of a high CMRR?
 5. How significant is the change in CMRR when using the improved current source? Based on the improvement, estimate the internal impedance of the current source.
-

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SECTION OVERVIEW

11.3: The Non-inverting Voltage Amplifier

Objective

In this exercise, the performance of the non-inverting voltage amplifier will be examined. The investigation will include the effect of feedback resistors on setting voltage gain, stability of gain with differing op amps, and input impedance.

[11.3.1: Theory Overview](#)

[11.3.2: Reference](#)

[11.3.3: Equipment](#)

[11.3.4: Components](#)

[11.3.5: Schematics](#)

[11.3.6: Procedure](#)

[11.3.7: Data Tables](#)

[11.3.8: Questions](#)

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11.3.1: Theory Overview

The non-inverting voltage amplifier is based on series-parallel negative feedback. As the ideal voltage-controlled voltage source, this amplifier exhibits high input impedance, low output impedance, and stable voltage gain. The voltage gain is set by the two feedback resistors, R_i and R_f .

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11.3.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 3.4, The Four Variants of Negative Feedback

Section 4.2, Inverting and Non-inverting Amplifiers

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11.3.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

4.3.1: For Distortion Measurement Only

(1) Low distortion sine source

model:_____ srn:_____

(1) Distortion analyzer

model:_____ srn:_____

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11.3.4: Components

(3) General purpose op amps (1 each of 741, 351, 318, 411, 081, etc.)

(2) $1\mu\text{F}$

actual: _____

(1) $1\text{k}\Omega$

actual: _____

(1) $4\text{k}7\Omega$

actual: _____

(1) $10\text{k}\Omega$

actual: _____

(1) $22\text{k}\Omega$

actual: _____

(1) $33\text{k}\Omega$

actual: _____

(1) $47\text{k}\Omega$

actual: _____

(1) $100\text{k}\Omega$

actual: _____

LM741 Datasheet: <http://www.ti.com/lit/ds/symlink/lm741.pdf>

LF351 Datasheet: <https://www.st.com/resource/en/datasheet/lf351.pdf>

LF411 Datasheet: <http://www.ti.com/lit/ds/symlink/lf411.pdf>

LM318 Datasheet: <http://www.ti.com/lit/ds/symlink/lm318-n.pdf>

TL081 Datasheet: <http://www.ti.com/lit/ds/symlink/tl081.pdf>

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11.3.5: Schematics

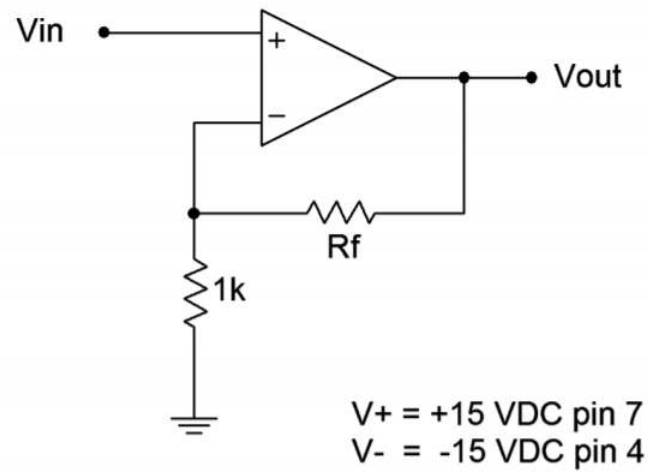


Figure 11.3.5.1

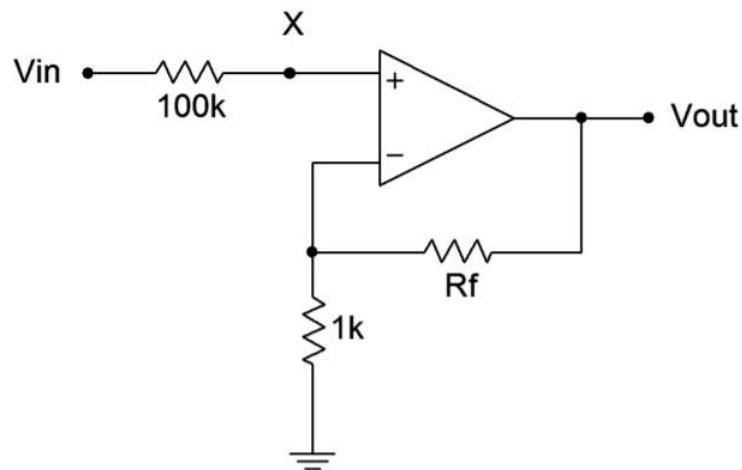


Figure 11.3.5.2

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11.3.6: Procedure

1. The voltage gain of the non-inverting amplifier can be determined accurately from the feedback resistors R_i and R_f . Calculate the voltage gains for the amplifier of Figure 4.5.1 for the R_f values specified, and record them in Table 4.7.1.
2. Assemble the circuit of Figure 4.5.1 using the 4k7 Ω resistor.
3. Set the generator to a 1 kHz sine wave, 100 millivolts peak.
4. Apply the generator to the amplifier. Measure and record the output voltage in Table 4.7.1. Also, compute the resulting experimental voltage gain and gain deviation.
5. Repeat step 4 for the remaining R_f values in Table 4.7.1.
6. For any given R_i , R_f combination, the voltage gain should be stable regardless of the precise op amp used, even if it is of an entirely different model. To verify this, first set R_f to 22k Ω .
7. Set the generator to a 1 kHz sine wave, 100 millivolts peak.
8. Apply the generator to the amplifier. Measure and record the output voltage in Table 4.7.2. Also, compute the resulting experimental voltage gain and gain deviation.
9. Repeat step 8 for two other op amps.
10. It is not practical to use an ohmmeter to determine the input impedance of an active circuit. Instead, input impedance can be found by utilizing the voltage divider effect. Modify the circuit by adding the extra input resistor as shown in Figure 4.5.2.
11. Set R_f to 4k7 Ω .
12. Set the generator to a 200 Hz sine wave, 1 volt peak.
13. Apply the generator to the amplifier. Use a DMM to measure and record the AC potential from V_{in} to point X (i.e., V_A , the voltage across the 100k) in Table 4.7.3. Using KVL, determine the voltage from point X to ground (V_B) and record in Table 4.7.3 (don't forget to compensate for peak versus RMS readings). Finally, compute the resulting input impedance by using the voltage divider rule. Note: If the DMM is not sensitive enough and registers 0 volts for V_A , it is safe to assume that Z_{in} is considerably larger than the 100k Ω sensing resistor.

4.6.1: Distortion Measurement

14. Return to the amplifier of Figure 4.5.1 with R_f set to 10k Ω . If available, the LF351 is a good choice for the op amp in this portion. Replace the general purpose generator with the low distortion sine source set to 1 kHz. Adjust its output level so that the output of the op amp is approximately 0 dBV.
15. Apply the distortion analyzer to the output of the op amp, read the resulting THD percentage and record it in Table 4.7.4.
16. Repeat steps 14 and 15 using the remaining R_f values in Table 4.7.4.

4.6.2: Troubleshooting

17. Continuing with the amplifier of Figure 4.5.1, reset R_f to 4k7 Ω . Estimate and then measure the results for each individual error presented in Table 4.7.5.

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11.3.7: Data Tables

R_f	Theoretical A_v	V_{out}	Experimental A_v	% Deviation
4k Ω				
10k Ω				
22k Ω				
33k Ω				
47k Ω				

Table 11.3.7.1

Op Amp	Theoretical A_v	V_{out}	Experimental A_v	% Deviation
1				
2				
3				

Table 11.3.7.2

V_A	V_B	Z_{in}

Table 11.3.7.3

R_f	% THD
10k Ω	
22k Ω	
47k Ω	

Table 11.3.7.4

Error	Quantity	Estimate	Actual
R_i 's third band is orange	V_{out}		
f_{in} is 100 Hz	V_{out}		
R_i is swapped with R_f	V_{out}		
+ and – signal input pins swapped	V_{out}		

Table 11.3.7.5

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11.3.8: Questions

1. What is the effect as R_f is increased?
 2. How does the voltage gain vary as the op amp is changed?
 3. Does the non-inverting voltage amplifier exhibit a predictable and stable voltage gain?
 4. What can be said about the input impedance of this type of amplifier?
 5. What is the relationship between gain, feedback and distortion?
-

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SECTION OVERVIEW

11.4: The Inverting Voltage Amplifier

Objective

In this exercise, the performance of the inverting voltage amplifier will be examined. The investigation will include the effect of feedback resistors on setting voltage gain, stability of gain with differing op amps, and the concept of virtual ground.

[11.4.1: Theory Overview](#)

[11.4.2: Reference](#)

[11.4.3: Equipment](#)

[11.4.4: Components](#)

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11.4.1: Theory Overview

The inverting voltage amplifier is based on parallel-parallel negative feedback. This amplifier exhibits modest input impedance, low output impedance, and stable inverting voltage gain. The voltage gain is set by the two feedback resistors, R_i and R_f .

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11.4.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 4.2, Inverting and Non-inverting Amplifiers

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11.4.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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11.4.4: Components

(3) General purpose op amps (1 each of 741, 351, 318, 411, 081, etc.)

(2) $1\mu\text{ F}$

actual: _____

(1) $1\text{ k } \Omega$

actual: _____

(1) $4\text{ k } 7 \Omega$

actual: _____

(1) $10\text{ k } \Omega$

actual: _____

(1) $22\text{ k } \Omega$

actual: _____

(1) $33\text{ k } \Omega$

actual: _____

(1) $47\text{ k } \Omega$

actual: _____

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11.4.5: Schematics

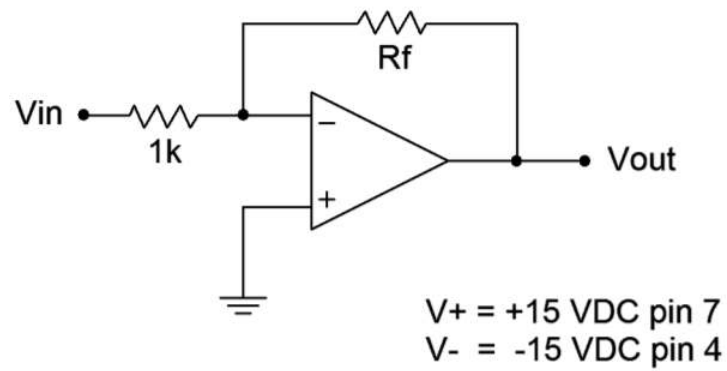


Figure 11.4.5.1

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11.4.6: Procedure

1. The voltage gain of the inverting amplifier can be determined accurately from the feedback resistors R_i and R_f . Calculate the voltage gains for the amplifier of Figure 5.5.1 for the R_f values specified, and record them in Table 5.7.1.
2. Assemble the circuit of Figure 5.5.1 using the 4k7 Ω resistor.
3. Set the generator to a 1 kHz sine wave, 100 millivolts peak.
4. Apply the generator to the amplifier. Measure and record the output voltage in Table 5.7.1, noting its phase relative to the input. Also, compute the resulting experimental voltage gain and gain deviation.
5. Repeat step 4 for the remaining R_f values in Table 5.7.1.
6. For any given R_i , R_f combination, the voltage gain should be stable regardless of the precise op amp used, even if it is of an entirely different model. To verify this, first set R_f to 22k Ω .
7. Set the generator to a 1 kHz sine wave, 100 millivolts peak.
8. Apply the generator to the amplifier. Measure and record the output voltage in Table 5.7.2. Also, compute the resulting experimental voltage gain and gain deviation.
9. Repeat step 8 for two other op amps.
10. The concept of virtual ground is very important. A virtual ground exists at the inverting input of the op amp in this circuit. Ideally, the voltage at this point should be very close to 0. Through voltage divider effect, this implies that all of the input signal must be dropping across R_i , and thus R_i must establish the input impedance of the amplifier.
11. Set R_f to 4k7 Ω .
12. Set the generator to a 200 Hz sine wave, 1 volt peak.
13. Apply the generator to the amplifier. Use a DMM to measure and record the AC potential at the inverting terminal of the op amp. Record the value in Table 5.7.3.

5.6.1: Computer Simulation

14. Build the circuit in a simulator and run a Transient Analysis echoing steps 2 through 5. Compare the results to the waveforms generated experimentally.
15. Repeat step 14 but this time use the Distortion Analyzer instrument to compare voltage gain to THD.

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11.4.7: Data Tables

R_f	A_v Theory	V_{out}'	Phase	Experimental A_v	% Deviation
4k7 Ω					
10k Ω					
22k Ω					
33k Ω					
47k Ω					

Table 11.4.7.1

Op Amp	A_v Theory	V_{out}	Experimental A_v	% Deviation
1				
2				
3				

Table 11.4.7.2

$V_{\text{inverting-input}} \setminus$	
--	--

Table 11.4.7.3

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11.4.8: Questions

1. What is the effect as R_f is increased?
 2. How does the voltage gain vary as the op amp is changed?
 3. Does the inverting voltage amplifier exhibit a predictable and stable voltage gain?
 4. What can be said about the input impedance of this type of amplifier?
 5. Based on the simulation, what is the relationship between gain, feedback and distortion for this circuit?
-

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SECTION OVERVIEW

11.5: The Op Amp Differential Amplifier

Objective

In this exercise, the performance of an op amp based differential amplifier will be examined. The investigation will include the effects of differential gain and common-mode rejection ratio (CMRR).

[11.5.1: Theory Overview](#)

[11.5.2: Reference](#)

[11.5.3: Equipment](#)

[11.5.4: Components](#)

[11.5.5: Schematics](#)

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11.5.1: Theory Overview

An op amp differential amplifier can be created by combining both a non-inverting voltage amplifier and an inverting voltage amplifier in a single stage. Proper gain matching between the two paths is essential to maximize the common-mode rejection ratio. Differential gain is equal to the gain of the inverting path.

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11.5.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 4.2, Inverting and Non-inverting Amplifiers

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11.5.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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11.5.4: Components

(2) General purpose op amps (741, 351, etc.)

(2) 1 μF

actual: _____

(2) 10 $\text{k}\Omega$

actual: _____

(1) 15 $\text{k}\Omega$

actual: _____

(1) 22 $\text{k}\Omega$

actual: _____

(2) 100 $\text{k}\Omega$

actual: _____

(1) 10 $\text{k}\Omega$ potentiometer

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11.5.5: Schematics

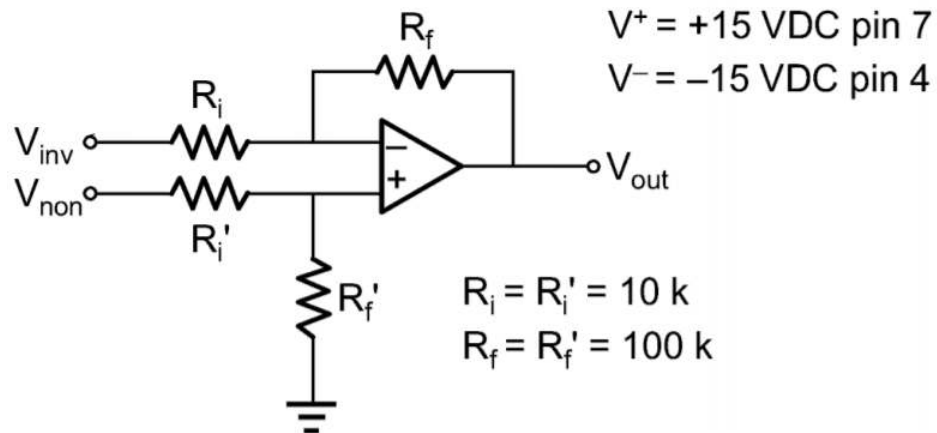


Figure 11.5.5.1

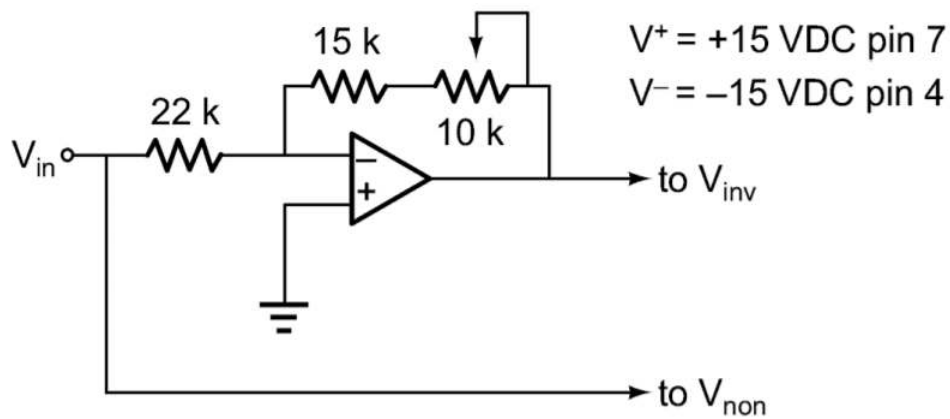


Figure 11.5.5.2

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11.5.6: Procedure

1. This circuit can be examined through the use of the Superposition Theorem. The contribution of each input can be measured individually, combined, and then compared with common-mode and differential inputs.
2. Calculate the differential voltage gain for the amplifier and record it in Table 6.7.1
3. Assemble the circuit of Figure 6.5.1. Try to get the R_i/R_f ratio as close as possible to the R_i'/R_f' ratio, even if you have to mix and match several resistors.
4. Set the generator to a 1 kHz sine wave, 500 millivolts peak.
5. Apply the generator to the V_{inv} input, and ground the V_{non} input.
6. Measure and record the output voltage in Table 6.7.2, noting the phase relative to the input. Also, compute the resulting voltage gain.
7. Swap the inputs by connecting the V_{non} input to the generator, and grounding the V_{inv} input.
8. Measure and record the output voltage in Table 6.7.2, noting the phase relative to the input. Also, compute the resulting voltage gain.
9. Compare the results of step 6 to step 8. The gains should be identical except that one is inverting while the other is non-inverting. Calculate the results of adding the two output signals and place the values in Table 6.7.3.
10. To measure the common-mode gain, connect both inputs to the generator (removing the V_{inv} ground). Record the output voltage and resulting gain in Table 6.7.3.
11. Assemble the circuit of Figure 6.5.2. Adjust the potentiometer to set the voltage gain to precisely -1 . This circuit is a simple phase-splitter and is used to generate a differential input signal.
12. Connect the circuit of Figure 6.5.2 to the original circuit as shown.
13. Measure and record the output voltage in Table 6.7.3.
14. Based on the results of Table 6.7.3, compute the experimental common-mode rejection ratio and place it in Table 6.7.4.

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11.5.7: Data Tables

Theoretical Differential Gain

Table 11.5.7.1

Input	V_{out}	Phase	A_v
V_{inv}			
V_{non}			

Table 11.5.7.1

Circuit	V_{out}	A_v
Superposition		
Common-mode		
Differential		

Table 11.5.7.1

Experimental CMRR

Table 11.5.7.1

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11.5.8: Questions

1. What controls the differential gain?
 2. Why is it important to match the resistor ratios in step 3?
 3. Why is it important to set the gain of the phase-splitter to precisely one in step 11?
 4. What determines the theoretical maximum CMRR for the op amp differential amplifier?
-

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