CIRCUITS AND ELECTRONICS LABORATORY



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Circuits & Electronics Laboratory

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Glossary

Detailed Licensing

Detailed Licensing

Licensing

*A detailed breakdown of this resource's licensing can be found in **Back Matter/Detailed Licensing**.*

CHAPTER OVERVIEW

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1.1: Lab Safety and Tools

If proper procedures are followed, the electrical lab is a perfectly safe place in which to work. There are some basic rules: No food or drink is allowed in lab at any time. Liquids are of particular danger as they are ordinarily conductive. While the circuitry used in lab is normally of no shock hazard, some of the test equipment may have very high internal voltages that could be lethal (in excess of 10,000 volts). Spilling a bottle of water or soda onto such equipment could leave the experimenter in the receiving end of a severe shock. Similarly, items such as books and jackets should not be left on top of the test equipment as it could cause overheating.

Each lab bench is self contained. All test equipment is arrayed along the top shelf. Beneath this shelf at the back of the work area is a power strip. All test equipment for this bench should be plugged into this strip. None of this equipment should be plugged into any other strip. This strip is controlled by a single circuit breaker which also controls the bench light. In the event of an emergency, all test equipment may be powered off through this one switch. Further, the benches are controlled by dedicated circuit breakers in the front of the lab. Next to this main power panel is an A/B/C class fire extinguisher suitable for electrical fires. Located at the rear of the lab is a safety kit. This contains bandages, cleaning swaps and the like for small cuts and the like. For serious injury, the Security Office will be contacted.

A lab bench should always be left in a secure mode. This means that the power to each piece of test equipment should be turned off, the bench itself should be turned off, all AC and DC power and signal sources should be turned down to zero, and all other equipment and components properly stowed with lab stools pushed under the bench.

It is important to come prepared to lab. This includes the class text, the lab exercise for that day, class notebook, calculator, and hand tools. The tools include an electronic breadboard, test leads, wire strippers, and needle-nose pliers or hemostats. A small pencil soldering iron may also be useful. A basic DMM (digital multimeter) rounds out the list.

A typical breadboard or protoboard is shown below:

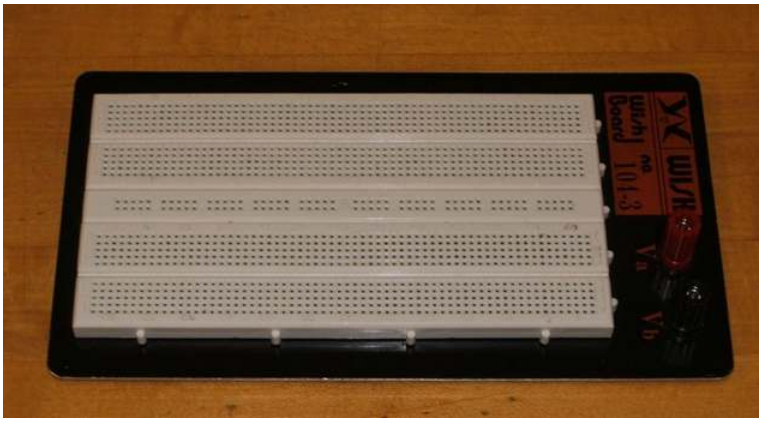


Figure 1.1.1

This particular unit features two main wiring sections with a common strip section down the center. Boards can be larger or smaller than this and may or may not have the mounting plate as shown. The connections are spaced 0.1 inch apart which is the standard spacing for many semiconductor chips. These are clustered in groups of five common terminals to allow multiple connections. The exception is the common strip which may have dozens of connection points. These are called buses and are designed for power and ground connections. Interconnections are normally made using small diameter solid hookup wire, usually AWG 22 or 24. Larger gauges may damage the board while smaller gauges do not always make good connections and are easy to break.

In the picture below, the color highlighted sections indicate common connection points. Note the long blue section which is a bus. This unit has four discrete buses available. When building circuits on a breadboard, it is important to keep the interconnecting wires short and the layout as neat as possible. This will aid both circuit functioning and ease of troubleshooting.

Examples of breadboard usage can be found in Appendix D. Be sure to read it!

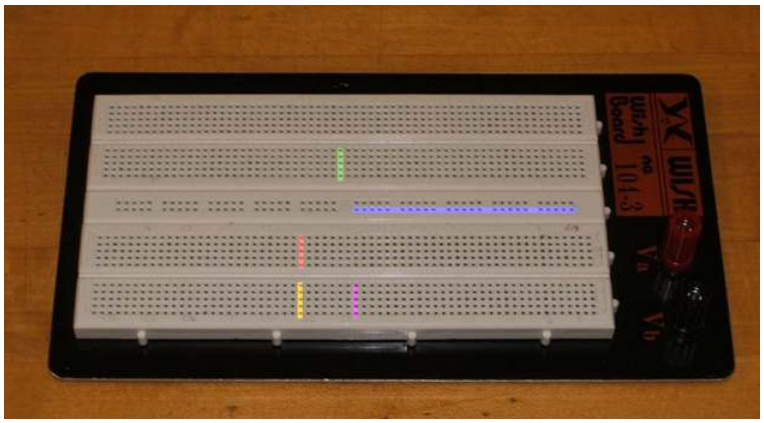


Figure 1.1.2

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1.2: Scientific and Engineering Notation

Scientists and engineers often work with very large and very small numbers. The ordinary practice of using commas and leading zeroes proves to be very cumbersome in this situation. Scientific notation is more compact and less error prone method of representation. The number is split into two portions: a precision part (the mantissa) and a magnitude part (the exponent, being a power of ten). For example, the value 23,000 could be written as 23 times 10 to the 3rd power (that is, times one thousand). The exponent may be thought of in terms of how places the decimal point is moved to the left. Spelling this out is awkward, so a shorthand method is used where “times 10 to the X power” is replaced by the letter E (which stands for exponent). Thus, 23,000 could be written as 23E3. The value 45,000,000,000 would be written as 45E9. Note that it would also be possible to write this number as 4.5E10 or even 0.45E11. The only difference between scientific notation and engineering notation is that for engineering notation the exponent is always a multiple of three. Thus, 45E9 is proper engineering notation but 4.5E10 isn’t. On most scientific calculators E is represented by either an “EE” or “EXP” button. The process of entering the value 45E9 would be depressing the keys 4 5 EE 9.

For fractional values, the exponent is negative and may be thought of in terms how many places the decimal point must be moved to the right. Thus, 0.00067 may be written as 0.67E−3 or 6.7E−4 or even 670E−6. Note that only the first and last of these three are acceptable as engineering notation.

Engineering notation goes one step further by using a set of prefixes to replace the multiples of three for the exponent. The prefixes are:

E12 = Tera (T)	E9 = Giga (G)	E6 = Mega (M)	E3 = kilo (k)
E−3 = milli (m)	E−6 = micro (μ)	E−9 = nano (n)	E−12 = pico (p)

Table 1.2.1

Thus, 23,000 volts could be written as 23E3 volts or simply 23 kilovolts.

Besides being more compact, this notation is much simpler than the ordinary form when manipulating wide ranging values. When multiplying, simply multiply the precision portions and add the exponents. Similarly, when dividing, divide the precision portions and subtract the exponents. For example, 23,000 times 0.000003 may appear to be a complicated task. In engineering notation this is 23E3 times 3E−6. The result is 69E−3 (that is, 0.069). Given enough practice it will become second nature that kilo (E3) times micro (E−6) yields milli (E−3). This will facilitate lab estimates a great deal. Continuing, 42,000,000 divided by 0.002 is 42E6 divided by 2E−3, or 21E9 (the exponent is 6 minus a negative 3, or 9).

When adding or subtracting, first make sure that the exponents are the same (scaling if required) and then add or subtract the precision portions. For example, 2E3 plus 5E3 is 7E3. By comparison, 2E3 plus 5E6 is the same as 2E3 plus 5000E3, or 5002E3 (or 5.002E6).

Perform the following operations. Convert the following into scientific and engineering notation.

1. 1,500

2. 63,200,000

3. 0.0234

4. 0.000059

5. 170

Convert the following into normal longhand notation:

6. 1.23E3

7. 54.7E6

8. 2E−3

9. 27E−9

10. 4.39E7

Use the appropriate prefix for the following:

11. 4E6 volts

12. 5.1E3 feet

13. 3.3E−6 grams

Perform the following operations:

14. 5.2E6 + 1.7E6

15. 12E3 − 900

16. 1.7E3 · 2E6

17. 48E3 / 4E6

18. 20 / 4E3

19. 10 M · 2 k

20. 8 n / 2 m

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1.3: Laboratory Reports

Unless specified otherwise, all lab exercises require a non-formal laboratory report. Lab reports are individual endeavors not group work. The deadline for reports is one week after the exercise is performed. A letter grade is subtracted for the first half-week late and two letter grades are subtracted for the second half-week late. Reports are not acceptable beyond one week late. A basic report should include a statement of the Objective (i.e., those items under investigation), a Conclusion (what was found or verified), a Discussion (an explanation and analysis of the lab data which links the Objective to the Conclusion), Data Tables and Graphs, and finally, answers to any problems or questions posed in the exercise. Details of the structure of the report along with an example report may be found in Appendices A, B and C.

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SECTION OVERVIEW

1.4: DC Sources and Metering

Objective

The objective of this exercise is to become familiar with the operation and usage of basic DC electrical laboratory devices, namely DC power supplies and digital multimeters.

1.4.1: Theory Overview

1.4.2: Equipment

1.4.3: Procedure

1.4.4: Data Tables

1.4.5: Questions

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1.4.1: Theory Overview

The adjustable DC power supply is a mainstay of the electrical and electronics laboratory. It is indispensible in the prototyping of electronic circuits and extremely useful when examining the operation of DC systems. Of equal importance is the handheld digital multimeter or DMM. This device is designed to measure voltage, current, and resistance at a minimum, although some units may offer the ability to measure other parameters such as capacitance or transistor beta. Along with general familiarity of the operation of these devices, it is very important to keep in mind that no measurement device is perfect; their relative accuracy, precision, and resolution must be taken into account. Accuracy refers to how far a measurement is from that parameter's true value. Precision refers to the repeatability of the measurement, that is, the sort of variance (if any) that occurs when a parameter is measured several times. For a measurement to be valid, it must be both accurate and repeatable. Related to these characteristics is resolution. Resolution refers to the smallest change in measurement that may be discerned. For digital measurement devices this is ultimately limited by the number of significant digits available to display.

A typical DMM offers 3 1/2 digits of resolution, the half-digit referring to a leading digit that is limited to zero or one. This is also known as a "2000 count display", meaning that it can show a minimum of 0000 and a maximum of 1999. The decimal point is "floating" in that it could appear anywhere in the sequence. Thus, these 2000 counts could range from 0.000 volts up to 1.999 volts, or 00.00 volts to 19.99 volts, or 000.0 volts to 199.9 volts, and so forth. With this sort of limitation in mind, it is very important to set the DMM to the lowest range that won't produce an overload in order to achieve the greatest accuracy.

A typical accuracy specification would be 1% of the reading plus two counts. "Reading" refers to the value displayed. If the 2 volt range was selected to read 1 volt (a measurement range of 0.000 to 1.999 for a 3 1/2 digit meter), 1% would be 10 millivolts (0.01 volts). To this a further uncertainty of two counts (i.e., the finest digit) must be included. In this example, the finest digit is one millivolt (0.001 volts) so this adds another 2 millivolts for a total of 12 millivolts of potential inaccuracy. In other words, the value displayed by the meter could be as much as 12 millivolts higher or lower than the true value. For the 20 volt range the inaccuracy would be computed in like manner but notice that accuracy is lost because the lowest digit is larger (i.e., the "counts" represent a larger value). In this case, the counts portion jumps up to 20 mV for a total inaccuracy of 30 mV. Obviously, if a signal in the vicinity of, say, 1.3 volts was to be measured, greater accuracy will be obtained on the 2 volt scale than on either the 20 or 200 volt scales. In contrast, the 200 millivolt scale would produce an overload situation and cannot be used. Overloads are often indicated by either a flashing display or a readout of "OL". Finally, analog meters typically give a base accuracy in terms of a percentage of "full scale" (i.e., the selected scale or range) and not the signal itself, and obviously, there is no "counts" specification.

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1.4.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) Precision digital multimeter

model:_____ srn:_____

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1.4.3: Procedure

1. Assume a general purpose 3 1/2 digit DMM is being used. Its base accuracy is listed as 2% of reading plus 5 counts. Compute the inaccuracy caused by the scale and count factors and determine the total for a full scale reading. Record these values in Table 2.4.1.

2. Repeat step one for a precision 4 1/2 digit DMM specified as 0.5% of reading plus 3 counts. Record the results in Table 2.4.2.

3. Set the adjustable power supply to 2.2 volts via its display. Use both the Coarse and Fine controls to get as close to 2.2 volts as possible. Record the displayed voltage in the first column of Table 2.4.3. Using the general purpose DMM set to the DC voltage function, set the range to 20 volts full scale. Measure the voltage at the output jacks of the power supply. Be sure to connect the DMM and power supply red lead to red lead, and black lead to black lead. Record the voltage registered by the DMM in the middle column of Table 2.4.3. Reset the DMM to the 200 volt scale, re-measure the voltage, and record in the final column

4. Repeat step three for the remaining voltages of Table 2.4.3.

5. Using the precision DMM, repeat steps three and four, recording the results in Table 2.4.4.

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1.4.4: Data Tables

Scale	2% Reading	5 Counts	Total
200 mV			
20 V			

Table 1.4.4.1

Scale	.5% Reading	3 Counts	Total
200 mV			
20 V			

Table 1.4.4.2

Voltage	Power Supply	DMM 20V Scale	DMM 200V Scale
2.2			
5.0			
9.65			
15.0			

Table 1.4.4.3

Voltage	Power Supply	DMM 20V Scale	DMM 200V Scale
2.2			
5.0			
9.65			
15.0			

Table 1.4.4.4

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1.4.5: Questions

1. For the general purpose DMM of Table 2.4.1, which contributes the larger share of inaccuracy; the full scale percentage or the count spec?

2. Bearing in mind that the power supply display is really just a very limited sort of digital volt meter, which voltages in Table 2.4.3 and 2.4.4 do you suspect to be the most accurately measured and why?

3. Assuming that the precision DMM used in Table 2.4.4 has a base accuracy spec of 0.1% plus 2 counts and is properly calibrated, what is the range of possible “true” voltages measured for 15.0 volts on the 20 volt scale?

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1.5: Component Identification

In this lab, many different electronic components are used including passive devices such as resistors and capacitors as well as semiconductors such as diodes and transistors, and finally, integrated circuits. These devices are available in many different case styles. Two broad classifications are through-hole and surface mount. As circuits will be built on protoboards, through-hole components are of particular interest here. Surface mount devices are generally smaller and use thin flat tabs or stubs in place of ordinary wire leads. In production they are soldered directly to the surface of the printed circuit board without the use of holes.

1.5.1 1.2.1: Resistors and Potentiometers

Resistors are perhaps the single most common component. They are classified as passive devices (versus active devices AKA semiconductors). Resistors have two leads and are not directional so they cannot be inserted backwards. Leads are usually axial (i.e., emanating from opposite ends). The physical size of a resistor indicates its power handling capacity, not its resistance. The general purpose lab resistor is usually a carbon film type, 1/4 watt dissipation. Resistance values are shown via a color coded series of bands for most types, although high precision resistors may have the value printed directly on the body.

Potentiometers may be either rotary or linear travel (slider), with rotary being the most common. Most rotary pots are 3/4 turn, although precision trim pots may be 20 turns or more. Typically, the center of the three connections is the wiper arm. Rotary pots may be designed for panel mount (for example, a volume control on a stereo) or board mount (such as a calibration control). The taper of a pot indicates how resistance and position are related. Pots may have a linear taper or a specialized audio taper (log taper). A linear taper means that a specific degree of rotation will produce the same resistance change. Rotating the shaft half way, for example, results in a 50/50 split of the resistance. In contrast, an audio taper pot would show a 10/90 split. Pots are also available in multi-gang, that is, several pots controlled by one common shaft.

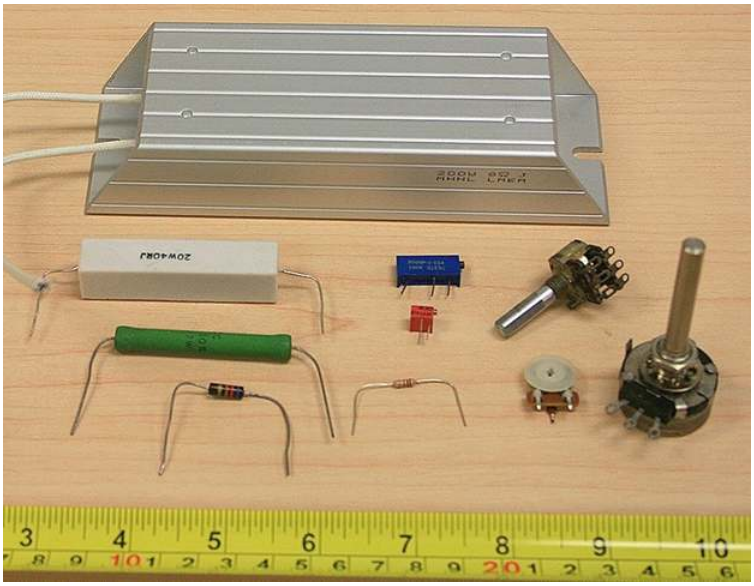


Figure 1.5.1: Resistors and Potentiometers Capacitors

1.5.2 1.2.2: Capacitors

are also classified as passives and can be though of as very short term energy storage devices. Capacitors are dual lead but may have either axial or radial (radiating from one end) leads. Unlike resistors, the physical size of a capacitor offers a clue as to its capacitance and voltage rating. All other factors being equal the greater the capacitance or voltage rating, the larger the capacitor. Most smaller capacitors (below 1 μF) are not polarized and can be inserted into a circuit either way. The more popular dielectrics for this range include the ceramics (usually disk or coin shaped) and poly film types (polyester, polypropylene, etc.) which are usually block shaped. Teardrop shaped tantalum capacitors are used commonly for power supply bypass. They are polarized and must be inserted in the circuit in the specified direction. Larger capacitance values (over 1 μF) are often realized via aluminum electrolytics. These are also polarized. Failure to insert these in the proper direction may result in unpredictable results, including

the capacitor exploding. While they do not perform as well as film types in terms of leakage, accuracy, etc., they are offer high volumetric efficiency (i.e., small physical size given the capacitance). Very large caps may have screw terminals in place of wire leads. In years past, color coding was common but this has generally been replaced with values printed directly on the body of the capacitor. Sometimes a numeric code is used such as “102”. This is read as 10 followed by 2 zeroes, with the result in picofarads, or 1000 pF (1 nF) in this case. Finally, because capacitors are charge storage devices, they may present a shock hazard from stored charge after they are removed from a circuit. This charge may be bled off with a low value resistance placed across the leads.

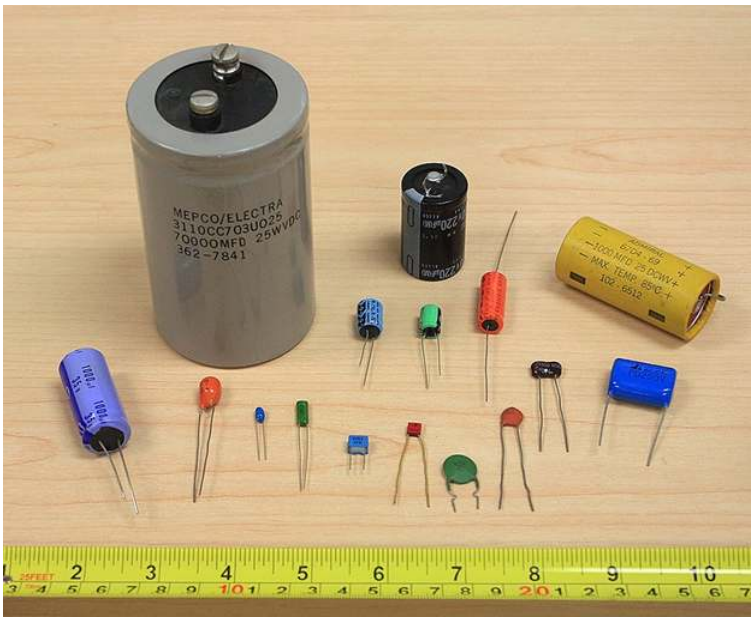


Figure 1.5.2: Capacitors

1.5.3 1.2.3: Inductors

The third and final passive device is the inductor. Also non-polarized, they normally have axial leads. Smaller values may be completely encapsulated and appear not much different from a carbon composition resistor. Others may use some form of jacket or coating while still others show bare wire (the wire only appears bare, it is in fact covered by a thin clear insulating coating). These vary from the size of small resistors to what appear to be large spools of wire.

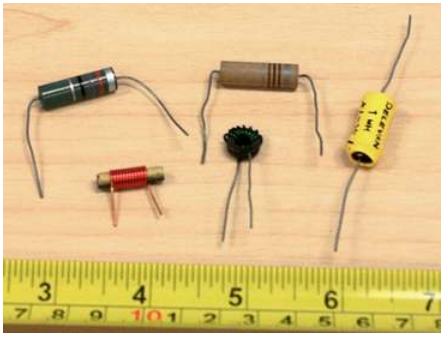


Figure 1.5.3: Inductors

1.5.4 1.2.4: Diodes

Diodes are a two lead semiconductor. They are polarized and typically have axial leads. The two leads are referred to as the anode and cathode. Signal diodes are around the size of 1/4 watt resistors and sometimes use a glass body. The cathode is marked by a band or stripe on the body of the diode. The cathode of an LED is usually marked by a flat spot on the plastic housing or by the shorter of the two leads. High power diodes are much more robust and might appear at first glance to be a short bolt or stud with leads attached to it. Component numbers are usually stamped on the body of the device.

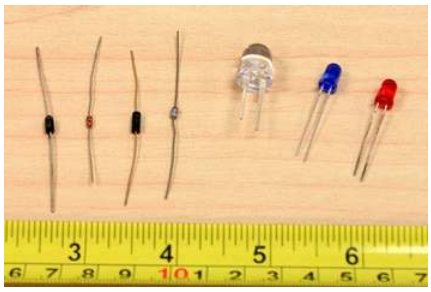


Figure 1.5.4: Diodes

1.5.5 1.2.5: Transistors

There are many types of transistors. Generally, they are three lead devices. Component model numbers will be stamped directly onto the case. Small power dissipation (< 500 mW) units will usually be seen in plastic TO-92 cases, round metal TO-5 cans or variations on the theme. Mid power devices typically use TO-220, TO-202 or the like “power tab” cases. For higher powers the oval TO-3 cases are employed. A similarly shaped but slightly smaller variant is the TO-66. Power devices will need to use a heat sink to keep them cool. TO-92 cases use a flattened front face so that the three pins may be distinguished from each other without confusion. The round TO-5 can uses a small tab to indicate pin 1.

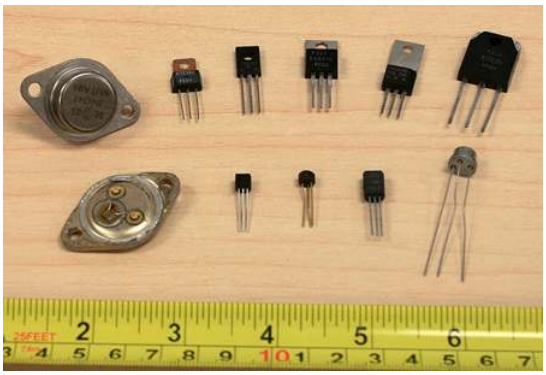


Figure 1.5.5: Transistors

1.5.6 1.2.6: Integrated Circuits

There are a very wide variety of integrated circuits. Multi-lead versions of the TO-5 can are sometimes used but the most common through-hole package is the Dual In-Line Package, denoted as DIP or DIL. A single in-line package is also available for some functions. High power devices often use multi-lead versions of the popular TO-220 and TO-3 case styles. Like other semiconductors, component model numbers are printed directly on the package. A notch or dimple will denote which lead is pin 1 on the DIP/DIL cases.

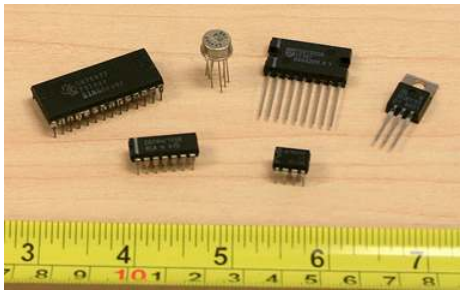


Figure 1.5.6: Integrated Circuits

1.5.7 1.2.7: Transformers

Transformers can vary from tiny audio devices to room size devices used in power generation and distribution. No matter the size, their job is a simple one: to isolate the source and load, to match two different impedance devices or to change the voltage level. A very common application is stepping down a 120 VAC line voltage to a more modest level so that it can be rectified, filtered, and turned into a stable DC source to drive electronic circuits. Besides the voltage turns ratio, the most important characteristic is the VA or volt-amps rating of the device. All other factors being equal, the higher the VA rating, the larger the transformer. Transformers applicable for consumer electronics may be either chassis mount with leads or PCB mount with through-hole pins. Transformers only operate with AC voltages.

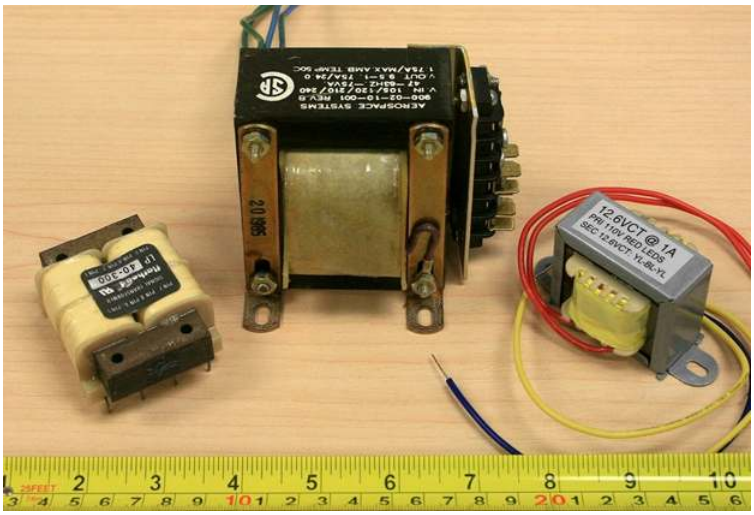


Figure 1.5.7: Transformers

1.5.8 1.2.8: Heat Sinks

Heat sinks are not a device, per se, but they are essential tools of semiconductor heat management. Their job is to effectively move heat from the semiconductor's case to the surrounding air, keeping the semiconductor cool. They range in size from small clip-ons to large extruded aluminum finned plates. Some cases, such as the body of the TO-3 or the tab of the TO-220 are electrically live. To prevent possible shorts and a live chassis, non-conductive isolating tabs and grommets are used to attach the semiconductors to the heat sink.

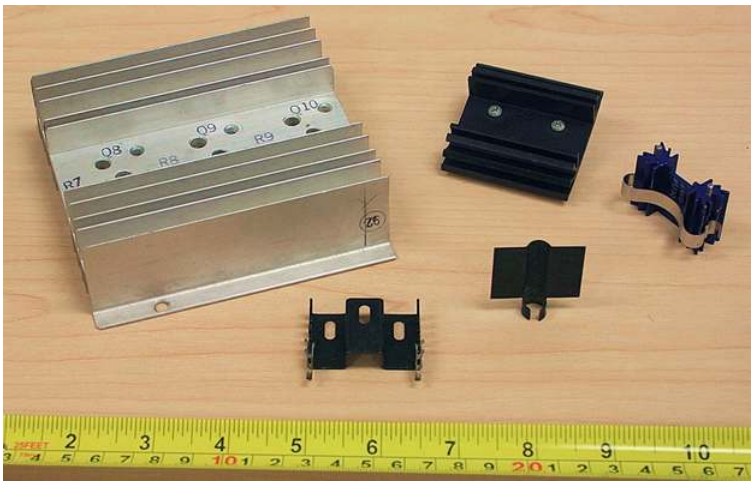


Figure 1.5.8: Heat Sinks

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CHAPTER OVERVIEW

2: Resistors

Objective

The objective of this exercise is to become familiar with the measurement of resistance values using a digital multimeter (DMM). A second objective is to learn the resistor color code.

2.1: Theory Overview
2.2: Equipment
2.3: Procedure
2.4: Data Tables
2.5: Questions
2.6: Ohm's Law
2.6.1: Theory Overview
2.6.2: Equipment
2.6.3: Schematic
2.6.4: Procedure
2.6.5: Data Tables
2.6.6: Questions

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2.1: Theory Overview

The resistor is perhaps the most fundamental of all electrical devices. Its fundamental attribute is the restriction of electrical current flow: The greater the resistance, the greater the restriction of current. Resistance is measured in ohms. The measurement of resistance in unpowered circuits may be performed with a digital multimeter. Like all components, resistors cannot be manufactured to perfection. That is, there will always be some variance of the true value of the component when compared to its nameplate or nominal value. For precision resistors, typically 1% tolerance or better, the nominal value is usually printed directly on the component. Normally, general purpose components, i.e. those worse than 1%, usually use a color code to indicate their value.

The resistor color code typically uses 4 color bands. The first two bands indicate the precision values (i.e. the mantissa) while the third band indicates the power of ten applied (i.e. the number of zeroes to add). The fourth band indicates the tolerance. It is possible to find resistors with five or six bands but they will not be examined in this exercise. Examples are shown below:

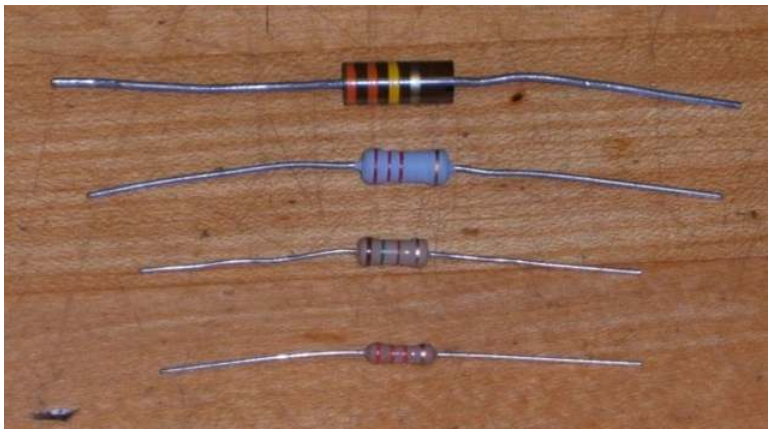


Figure 2.1.1

It is important to note that the physical size of the resistor indicates its power dissipation rating, not its ohmic value.

Each color in the code represents a numeral. It starts with black and finishes with white, going through the rainbow in between:

0 Black	1 Brown	2 Red	3 Orange	4 Yellow
5 Green	6 Blue	7 Violet	8 Gray	9 White

Table 2.1.1

For the fourth, or tolerance, band:

5% Gold	10% Silver	20% None

Table 2.1.2

For example, a resistor with the color code brown-red-orange-silver would correspond to 1 2 followed by 3 zeroes, or 12,000 ohms (more conveniently, 12 k ohms). It would have a tolerance of 10% of 12 k ohms or 1200 ohms. This means that the actual value of any particular resistor with this code could be anywhere between 12,000 − 1200=10,800, to 12,000 + 1200=13,200. That is, 10.8 k to 13.2 k ohms. Note, the IEC standard replaces the decimal point with the engineering prefix, thus 1.2 k is alternately written 1k2.

Similarly, a 470 k 5% resistor would have the color code yellow-violet-yellow-gold. To help remember the color code many mnemonics have been created using the first letter of the colors to create a sentence. One example is the picnic mnemonic Black Bears Robbed Our Yummy Goodies Beating Various Gray Wolves.

Measurement of resistors with a DMM is a very straight forward process. Simply set the DMM to the resistance function and choose the first scale that is higher than the expected value. Clip the leads to the resistor and record the resulting value.

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2.2: Equipment

(1) Digital multimeter

model:_____ srn:_____

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2.3: Procedure

1. Given the nominal values and tolerances in Table 3.4.1, determine and record the corresponding color code bands.

2. Given the color codes in Table 3.4.2, determine and record the nominal value, tolerance and the minimum and maximum acceptable values.

3. Obtain a resistor equal to the first value listed in Table 3.4.3. Determine the minimum and maximum acceptable values based on the nominal value and tolerance. Record these values in Table 3.4.3. Using the DMM, measured the actual value of the resistor and record it in Table 3.4.3. Determine the deviation percentage of this component and record it in Table 3.4.3. The deviation percentage may be found via: Deviation = 100 * (measured − nominal)/nominal. Circle the deviation if the resistor is out of tolerance.

4. Repeat Step 3 for the remaining resistor in Table 3.4.3.

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2.4: Data Tables

Value	Band 1	Band 2	Band 3	Band 4
27 @ 10%				
56 @ 10%				
180 @ 5%				
390 @ 10%				
680 @ 5%				
1.5 k @ 20%				
3.6 k @ 10%				
7.5 k @ 5%				
10 k @ 5%				
47 k @ 10%				
820 k @ 10%				
2.2 M @ 20 %				

Table 2.4.1

Colors	Nominal	Tolerance	Minimum	Maximum
red-red-black-silver				
blue-gray-black-gold				
brown-green-brown-gold				
orange-orange-brown-silver				
green-blue-brown –gold				
brown-red-red–silver				
red-violet-red–silve				
gray-red-red–gold				
brown-black-orange–gold				
orange-orange-orange–silver				
blue-gray-yellow–none				
green-black-green-silver				

Table 2.4.2

Value	Minimum	Maximum	Measured	Deviation
22 @ 10%				
68 @ 5%				
150 @ 5%				
330 @ 10%				
560 @ 5%				
1.2 k @ 5%				
2.7 k @ 10%				
8.2 k @ 5%				
10 k @ 5%				
33 k @ 10%				
680 k @ 10%				
5 M @ 20 %				

Table 2.4.3

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2.5: Questions

1. What is the largest deviation in Table 3.4.3? Would it ever be possible to find a value that is outside the stated tolerance? Why or why not?

2. If Steps 3 and 4 were to be repeated with another batch of resistors, would the final two columns be identical to the original Table 3.4.3? Why or why not?

3. Do the measured values of Table 3.4.3 represent the exact values of the resistors tested? Why or why not?

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SECTION OVERVIEW

2.6: Ohm’s Law

Objective

This exercise examines Ohm’s law, one of the fundamental laws governing electrical circuits. It states that voltage is equal to the product of current times resistance.

2.6.1: Theory Overview

2.6.2: Equipment

2.6.3: Schematic

2.6.4: Procedure

2.6.5: Data Tables

2.6.6: Questions

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2.6.1: Theory Overview

Ohm’s law is commonly written as V = I * R. That is, for a given current, an increase in resistance will result in a greater voltage. Alternately, for a given voltage, an increase in resistance will produce a decrease in current. As this is a first order linear equation, plotting current versus voltage for a fixed resistance will yield a straight line. The slope of this line is the conductance, and conductance is the reciprocal of resistance. Therefore, for a high resistance, the plot line will appear closer to the horizontal while a lower resistance will produce a more vertical plot line.

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2.6.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 1 kΩ resistor

_____

(1) 6.8 kΩ resistor

_____

(1) 33 kΩ resistor

_____

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2.6.3: Schematic

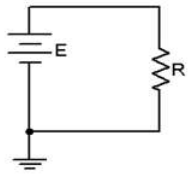


Figure 2.6.3.1

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2.6.4: Procedure

1. Build the circuit of Figure 4.1 using the 1 kΩ resistor. Set the DMM to measure DC current and insert it in-line between the source and resistor. Set the source for zero volts. Measure and record the current in Table 4.5.1. Note that the theoretical current is 0 and any measured value other than 0 would produce an undefined percent deviation.

2. Setting E at 2 volts, determine the theoretical current based on Ohm's law and record this in Table 4.5.1. Measure the actual current, determine the deviation, and record these in Table 4.5.1. Note that Deviation = 100 * (measured − theory) / theory.

3. Repeat step 2 for the remaining source voltages in Table 4.5.1.

4. Remove the 1 kΩ and replace it with the 6.8 kΩ. Repeat steps 1 through 3 using Table 4.5.2.

5. Remove the 6.8 kΩ and replace it with the 33 kΩ. Repeat steps 1 through 3 using Table 4.5.3.

6. Using the measured currents from Tables 4.5.1, 4.5.2, and 4.5.3, create a plot of current versus voltage. Plot all three curves on the same graph. Voltage is the horizontal axis and current is the vertical axis.

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2.6.5: Data Tables

E (volts)	I theory	I measured	Deviation
0	0		
2			
4			
6			
8			
10			
12			

Table 2.6.5.1 (1 kΩ)

E (volts)	I theory	I measured	Deviation
0	0		
2			
4			
6			
8			
10			
12			

Table 2.6.5.1 (6.8 kΩ)

E (volts)	I theory	I measured	Deviation
0	0		
2			
4			
6			
8			
10			
12			

Table 2.6.5.1 (33 kΩ)

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2.6.6: Questions

1. Does Ohm’s law appear to hold in this exercise?

2. Is there a linear relationship between current and voltage?

3. What is the relationship between the slope of the plot line and the circuit resistance?

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CHAPTER OVERVIEW

3: Resistor Combinations

3.1: Series DC Circuits
3.1.1: Theory Overview
3.1.2: Equipment
3.1.3: Schematics
3.1.4: Procedure
3.1.5: Data Tables
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SECTION OVERVIEW

3.1: Series DC Circuits

Objective

The focus of this exercise is an examination of basic series DC circuits with resistors. A key element is Kirchhoff's voltage law which states that the sum of voltage rises around a loop must equal the sum of the voltage drops. The voltage divider rule will also be investigated.

3.1.1: Theory Overview

3.1.2: Equipment

3.1.3: Schematics

3.1.4: Procedure

3.1.5: Data Tables

3.1.6: Questions

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3.1.1: Theory Overview

A series circuit is defined by a single loop in which all components are arranged in daisy-chain fashion. The current is the same at all points in the loop and may be found by dividing the total voltage source by the total resistance. The voltage drops across any resistor may then be found by multiplying that current by the resistor value. Consequently, the voltage drops in a series circuit are directly proportional to the resistance. An alternate technique to find the voltage is the voltage divider rule. This states that the voltage across any resistor (or combination of resistors) is equal to the total voltage source times the ratio of the resistance of interest to the total resistance.

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3.1.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 1 kΩ

_____

(1) 2.2 kΩ

_____

(1) 3.3 kΩ

_____

(1) 6.8 kΩ

_____

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3.1.3: Schematics

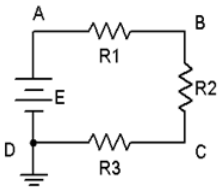


Figure 3.1.3.1

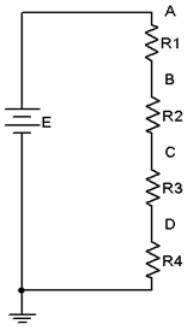


Figure 3.1.3.2

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3.1.4: Procedure

1. Using the circuit of Figure 5.3.1 with R1 = 1 k, R2 = 2.2 k, R3 = 3.3 k, and E = 10 volts, determine the theoretical current and record it in Table 5.5.1. Construct the circuit. Set the DMM to read DC current and insert it in the circuit at point A. Remember, ammeters go in-line and require the circuit to be opened for proper measurement. The red lead should be placed closer to the positive source terminal. Record this current in Table 5.5.1. Repeat the current measurements at points B and C.

2. Using the theoretical current found in Step 1, apply Ohm's law to determine the expected voltage drops across R1, R2, and R3. Record these values in the Theory column of Table 5.5.2.

3. Set the DMM to measure DC voltage. Remember, unlike current, voltage is measured across components. Place the DMM probes across R1 and measure its voltage. Again, red lead should be placed closer to the positive source terminal. Record this value in Table 5.5.2. Repeat this process for the voltages across R2 and R3. Determine the percent deviation between theoretical and measured for each of the three resistor voltages and record these in the final column of Table 5.5.2.

4. Consider the circuit of Figure 5.3.2 with R1 = 1 k, R2 = 2.2 k, R3 = 3.3 k, R4 = 6.8 k and E = 20 volts. Using the voltage divider rule, determine the voltage drops across each of the four resistors and record the values in Table 5.5.3 under the Theory column. Note that the larger the resistor, the greater the voltage should be. Also determine the potentials V_{AC} and V_B, again using the voltage divider rule.

5. Construct the circuit of Figure 5.3.2 with R1 = 1 k, R2 = 2.2 k, R3 = 3.3 k, R4 = 6.8 k and E = 20 volts. Set the DMM to measure DC voltage. Place the DMM probes across R1 and measure its voltage. Record this value in Table 5.5.3. Also determine the deviation. Repeat this process for the remaining three resistors.

6. To find V_{AC}, place the red probe on point A and the black probe on point C. Similarly, to find V_B, place the red probe on point B and the black probe on ground. Record these values in Table 5.5.3 with deviations.

3.1.4.1 5.4.1: Simulation

7. Build the circuit of Figure 5.3.1 in a simulator. Using the virtual DMM as a voltmeter determine the voltages at nodes A, B and C, and compare these to the theoretical and measured values recorded in Table 5.5.2.

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3.1.5: Data Tables

I Theory	I Point A	I Point B	I Point C

Table 3.1.5.1

Voltage	Theory	Measured	Deviation
R1			
R2			
R3			

Table 3.1.5.2

Voltage	Theory	Measured	Deviation
R1			
R2			
R3			
R4			
V_{AC}			
V_B			

Table 3.1.5.3

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3.1.6: Questions

1. For the circuit of Figure 5.3.1, what is the expected current measurement at point D?

2. For the circuit of Figure 5.3.2, what are the expected current and voltage measurements at point D?

3. In Figure 5.3.2, R4 is approximately twice the size of R3 and about three times the size of R2. Would the voltages exhibit the same ratios? Why/why not? What about the currents through the resistors?

4. If a fifth resistor of 10 kΩ was added below R4 in Figure 5.3.2, how would this alter V_{AC} and V_B? Show work.

5. Is KVL satisfied in Tables 5.5.2 and 5.5.3?

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SECTION OVERVIEW

3.2: Parallel DC Circuits

Objective

The focus of this exercise is an examination of basic parallel DC circuits with resistors. A key element is Kirchhoff's current law which states that the sum of currents entering a node must equal the sum of the currents exiting that node. The current divider rule will also be investigated.

3.2.1: Theory Overview

3.2.2: Equipment

3.2.3: Schematics

3.2.4: Procedure

3.2.5: Data Tables

3.2.6: Questions

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3.2.1: Theory Overview

A parallel circuit is defined by the fact that all components share two common nodes. The voltage is the same across all components and will equal the applied source voltage. The total supplied current may be found by dividing the voltage source by the equivalent parallel resistance. It may also be found by summing the currents in all of the branches. The current through any resistor branch may be found by dividing the source voltage by the resistor value. Consequently, the currents in a parallel circuit are inversely proportional to the associated resistances. An alternate technique to find a particular current is the current divider rule. For a two resistor circuit this states that the current through one resistor is equal to the total current times the ratio of the other resistor to the total resistance.

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3.2.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 1 kΩ

_____

(1) 2.2 kΩ

_____

(1) 3.3 kΩ

_____

(1) 6.8 kΩ

_____

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3.2.3: Schematics

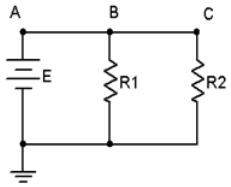


Figure 3.2.3.1

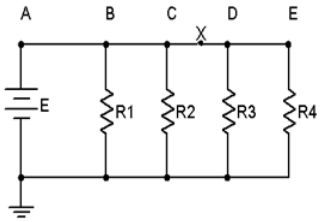


Figure 3.2.3.2

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3.2.4: Procedure

1. Using the circuit of Figure 6.3.1 with R1 = 1 k, R2 = 2.2 k and E = 8 volts, determine the theoretical voltages at points A, B, and C with respect to ground. Record these values in Table 6.5.1. Construct the circuit. Set the DMM to read DC voltage and apply it to the circuit from point A to ground. The red lead should be placed at point A and the black lead should be connected to ground. Record this voltage in Table 6.5.1. Repeat the measurements at points B and C.

2. Apply Ohm's law to determine the expected currents through R1 and R2. Record these values in the Theory column of Table 6.5.2. Also determine and record the total current.

3. Set the DMM to measure DC current. Remember, current is measured at a single point and requires the meter to be inserted in-line. To measure the total supplied current place the DMM between points A and B. The red lead should be placed closer to the positive source terminal. Record this value in Table 6.5.2. Repeat this process for the currents through R1 and R2. Determine the percent deviation between theoretical and measured for each of the currents and record these in the final column of Table 6.5.2.

4. Crosscheck the theoretical results by computing the two resistor currents through the current divider rule. Record these in Table 6.5.3.

5. Consider the circuit of Figure 6.3.2 with R1 = 1 k, R2 = 2.2 k, R3 = 3.3 k, R4 = 6.8 k and E = 10 volts. Using the Ohm's law, determine the currents through each of the four resistors and record the values in Table 6.5.4 under the Theory column. Note that the larger the resistor, the smaller the current should be. Also determine and record the total supplied current and the current I_X. Note that this current should equal the sum of the currents through R3 and R4.

6. Construct the circuit of Figure 6.3.2 with R1 = 1 k, R2 = 2.2 k, R3 = 3.3 k, R4 = 6.8 k and E = 10 volts. Set the DMM to measure DC current. Place the DMM probes in-line with R1 and measure its current. Record this value in Table 6.5.4. Also determine the deviation. Repeat this process for the remaining three resistors. Also measure the total current supplied by the source by inserting the ammeter between points A and B.

7. To find I_X, insert the ammeter at point X with the black probe closer to R3. Record this value in Table 6.5.4 with deviation.

3.2.4.1 6.4.1: Simulation

8. Build the circuit of Figure 6.3.2 in a simulator. Using the virtual DMM as an ammeter determine the currents through the four resistors along with I_X, and compare these to the theoretical and measured values recorded in Table 6.5.4.

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3.2.5: Data Tables

Voltage	Theory	Measured
V_A		
V_B		
V_C		

Table 3.2.5.1

Current	Theory	Measured	Deviation
R1			
R2			
Total			

Table 3.2.5.2

Current	CDR Theory
R1	
R2	
Total	

Table 3.2.5.3

Current	Theory	Measured	Deviation
R1			
R2			
R3			
R4			
Total			
I_X			

Table 3.2.5.4

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3.2.6: Questions

1. For the circuit of Figure 6.3.1, what is the expected current entering the negative terminal of the source?

2. For the circuit of Figure 6.3.2, what is the expected current between points B and C?

3. In Figure 6.3.2, R4 is approximately twice the size of R3 and about three times the size of R2. Would the currents exhibit the same ratios? Why/why not?

4. If a fifth resistor of 10 kΩ was added to the right of R4 in Figure 6.3.2, how would this alter I_{Total} and I_X? Show work.

5. Is KCL satisfied in Tables 6.5.2 and 6.5.4?

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SECTION OVERVIEW

3.3: Series-Parallel DC Circuits

Objective

This exercise will involve the analysis of basic series-parallel DC circuits with resistors. The use of simple series-only and parallel-only sub-circuits is examined as one technique to solve for desired currents and voltages.

3.3.1: Theory Overview

3.3.2: Equipment

3.3.3: Schematics

3.3.4: Procedure

3.3.5: Data Tables

3.3.6: Questions

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3.3.1: Theory Overview

Simple series-parallel networks may be viewed as interconnected series and parallel sub-networks. Each of these sub-networks may be analyzed through basic series and parallel techniques such as the application of voltage divider and current divider rules along with Kirchhoff's voltage and current laws. It is important to identify the most simple series and parallel connections in order to jump to more complex interconnections.

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3.3.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 1 kΩ

_____

(1) 2.2 kΩ

_____

(1) 3.3 kΩ

_____

(1) 4.7 kΩ

_____

(1) 6.8 kΩ

_____

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3.3.3: Schematics

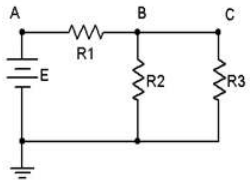


Figure 3.3.3.1

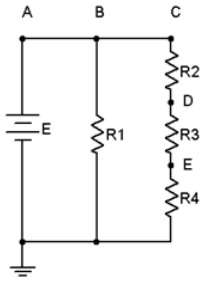


Figure 3.3.3.2

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3.3.4: Procedure

1. Consider the circuit of Figure 7.3.1 with R1 = 1 k, R2 = 2.2 k, R3 = 4.7 k and E = 10 volts. R2 is in parallel with R3. This combination is in series with R1. Therefore, the R2, R3 pair may be treated as a single resistance to form a series loop with R1. Based on this observation, determine the theoretical voltages at points A, B, and C with respect to ground. Record these values in Table 7.5.1. Construct the circuit. Set the DMM to read DC voltage and apply it to the circuit from point A to ground. Record this voltage in Table 7.5.1. Repeat the measurements at points B and C, determine the deviations, and record the values in Table 7.5.1.

2. Applying KCL to the parallel sub-network, the current entering node B (i.e., the current through R1) should equal the sum of the currents flowing through R2 and R3. These currents may be determined through Ohm's law and/or the current divider rule. Compute these currents and record them in Table 7.5.2. Using the DMM as an ammeter, measure these three currents and record the values along with deviations in Table 7.5.2.

3. Consider the circuit of Figure 7.3.2. R2, R3 and R4 create a series sub-network. This sub-network is in parallel with R1. By observation then, the voltages at nodes A, B and C should be identical as in any parallel circuit of similar construction. Due to the series connection, the same current flows through R2, R3 and R4. Further, the voltages across R2, R3 and R4 should sum up to the voltage at node C, as in any similarly constructed series network. Finally, via KCL, the current exiting the source must equal the sum of the currents entering R1 and R2.

4. Build the circuit of Figure 7.3.2 with R1 = 3.3 k, R2 = 2.2 k, R3 = 4.7 k, R4 = 6.8 k and E = 20 volts. Using the series and parallel relations noted in Step 3, calculate the voltages at points B, C, D and E. Measure these potentials with the DMM, determine the deviations, and record the values in Table 7.5.3.

5. Calculate the currents leaving the source and flowing through R1 and R2. Record these values in Table 7.5.4. Using the DMM as an ammeter, measure those same currents, compute the deviations, and record the results in Table 7.5.4.

3.3.4.1 7.4.1: Simulation

6. Build the circuit of Figure 7.3.1 in a simulator. Using the virtual DMM as a voltmeter determine the voltages at nodes A, B and C, and compare these to the theoretical and measured values recorded in Table 7.5.1.

7. Build the circuit of Figure 7.3.2 in a simulator. Using the DC Operating Point simulation function, determine the voltages at nodes B, C, D and E, and compare these to the theoretical and measured values recorded in Table 7.5.3.

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3.3.5: Data Tables

Voltage	Theory	Measured	Deviation
V_A			
V_B			
V_C			

Table 3.3.5.1

Current	Theory	Measured	Deviation
R_1			
R_2			
R_3			

Table 3.3.5.2

Voltage	Theory	Measured	Deviation
V_B			
V_C			
V_D			
V_E			

Table 3.3.5.3

Current	Theory	Measured	Deviation
Source			
R_1			
R_2			

Table 3.3.5.4

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3.3.6: Questions

1. Are KVL and KCL satisfied in Tables 7.5.1 and 7.5.2?

2. Are KVL and KCL satisfied in Tables 7.5.3 and 7.5.4?

3. How would the voltages at A and B in Figure 7.3.1 change if a fourth resistor equal to 10 k was added in parallel with R3? What if this resistor was added in series with R3?

4. How would the currents through R1 and R2 in Figure 7.3.2 change if a fifth resistor equal to 10 k was added in series with R1? What if this resistor was added in parallel with R1?

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SECTION OVERVIEW

3.4: Ladders and Bridges

Objective

The objective of this exercise is to continue the exploration of basic series-parallel DC circuits. The basic ladder network and bridge are examined. A key element here is the concept of loading, that is, the effect that a sub-circuit may have on a neighboring sub-circuit.

3.4.1: Theory Overview

3.4.2: Equipment

3.4.3: Schematics

3.4.4: Procedure

3.4.5: Data Tables

3.4.6: Questions

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3.4.1: Theory Overview

Ladder networks are comprised of a series of alternating series and parallel connections. Each section effectively loads the prior section, meaning that the voltage and current of the prior section may change considerably if the loading section is removed. One possible technique for the solution of ladder networks is a series of cascading voltage dividers. Current dividers may also be used. In contrast, bridge networks typically make use of four elements arranged in dual series and parallel configuration. These are often used in measurement systems with the voltage of interest derived from the difference of two series subcircuit voltages. As in the simpler series-parallel networks; KVL, KCL, the current divider rule and the voltage divider rule may be used in combination to analyze the sub-circuits.

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3.4.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 1 kΩ

_____

(1) 2.2 kΩ

_____

(1) 3.3 kΩ

_____

(1) 6.8 kΩ

_____

(1) 10 kΩ

_____

(1) 22 kΩ

_____

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3.4.3: Schematics

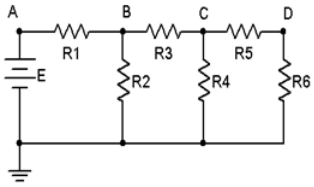


Figure 3.4.3.1

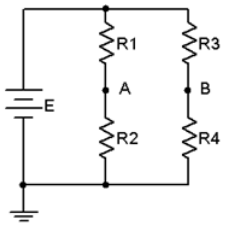


Figure 3.4.3.2

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3.4.4: Procedure

1. Consider the circuit of Figure 8.3.1. R5 and R6 form a simple series connection. Together, they are in parallel with R4. Therefore the voltage across R4 must be the same as the sum of the voltages across R5 and R6. Similarly, the current entering node C from R3 must equal the sum of the currents flowing through R4 and R5. This three resistor combination is in series with R3 in much the same manner than R6 is in series with R5. These four resistors are in parallel with R2, and finally, these five resistors are in series with R1. Note that to find the voltage at node B the voltage divider rule may be used, however, it is important to note that VDR cannot be used in terms of R1 versus R2. Instead, R1 reacts against the entire series-parallel combination of R2 through R6. Similarly, R3 reacts against the combination of R4, R5 and R6. That is to say R5 and R6 load R4, and R3 through R6 load R2. Because of this process note that V_D must be less than V_C, which must be less than V_B, which must be less than V_A. Thus the circuit may be viewed as a sequence of loaded voltage dividers.

2. Construct the circuit of Figure 8.3.1 using R1 = 1 k, R2 = 2.2 k, R3 = 3.3 k, R4 = 6.8 k, R5 = 10 k, R6 = 22 k and E = 20 volts. Based on the observations of Step 1, determine the theoretical voltages at nodes A, B, C and D, and record them in Table 8.5.1. Measure the potentials with a DMM, compute the deviations and record the results in Table 8.5.1.

3. Based on the theoretical voltages found in Table 8.5.1, determine the currents through R1, R2, R4 and R6. Record these values in Table 8.5.2. Measure the currents with a DMM, compute the deviations and record the results in Table 8.5.2.

4. Consider the circuit of Figure 8.3.2. In this bridge network, the voltage of interest is V_{AB}. This may be directly computed from $V_A - V_B$. Assemble the circuit using R1 = 1 k, R2 = 2.2 k, R3 = 10 k, R4 = 6.8 k and E = 10 volts. Determine the theoretical values for V_A, V_B and V_{AB} and record them in Table 8.5.3. Note that the voltage divider rule is very effective here as the R1 R2 branch and the R3 R4 branch are in parallel and therefore both “see” the source voltage.

5. Use the DMM to measure the potentials at A and B with respect to ground, the red lead going to the point of interest and the black lead going to ground. To measure the voltage from A to B, the red lead is connected to point A while the black is connected to point B. Record these potentials in Table 8.5.3. Determine the deviations and record these in Table 8.5.3.

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3.4.5: Data Tables

Voltage	Theory	Measured	Deviation
V_A			
V_B			
V_C			
V_D			

Table 3.4.5.1

Current	Theory	Measured	Deviation
R_1			
R_2			
R_4			
R_6			

Table 3.4.5.2

Voltage	Theory	Measured	Deviation
V_A			
V_B			
V_AB			

Table 3.4.5.3

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3.4.6: Questions

1. In Figure 8.3.1, if another pair of resistors was added across R6, would V_D go up, down, or stay the same? Why?

2. In Figure 8.3.1, if R4 was accidentally opened would this change the potentials at B, C and D? Why or why not?

3. If the DMM leads are reversed in Step 5, what happens to the measurements in Table 8.5.3?

4. Suppose that R3 and R4 are accidentally swapped in Figure 8.3.2. What is the new V_{AB}?

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SECTION OVERVIEW

3.5: Potentiometers and Rheostats

Objectives

The objective of this exercise is to examine the practical workings of adjustable resistances, namely the potentiometer and rheostat. Their usage in adjustable voltage and current control will be investigated.

3.5.1: Theory Overview

3.5.2: Equipment

3.5.3: Schematics

3.5.4: Procedure

3.5.5: Data Tables

3.5.6: Questions

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3.5.1: Theory Overview

A potentiometer is a three terminal resistive device. The outer terminals present a constant resistance which is the nominal value of the device. A third terminal, called the wiper arm, is in essence a contact point that can be moved along the resistance. Thus, the resistance seen from one outer terminal to the wiper plus the resistance from the wiper to the other outer terminal will always equal the nominal resistance of the device. This three terminal configuration is used typically to adjust voltage via the voltage divider rule, hence the name potentiometer, or pot for short. While the resistance change is often linear with rotation (i.e., rotating the shaft 50% yields 50% resistance), other schemes, called tapers, are also found. One common non-linear taper is the logarithmic taper. It is important to note that linearity can be compromised (sometimes on purpose) if the resistance loading the potentiometer is not significantly larger in value than the potentiometer itself.

If only a single outer terminal and the wiper are used, the device is merely an adjustable resistor and is referred to as a rheostat. These may be placed in-line with a load to control the load current, the greater the resistance, the smaller the current.

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3.5.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 10 kΩ potentiometer

(1) 100 kΩ potentiometer

(1) 1 kΩ

_____

(1) 4.7 kΩ

_____

(1) 47 kΩ

_____

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3.5.3: Schematics

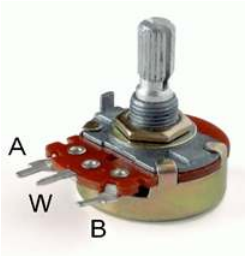


Figure 3.5.3.1

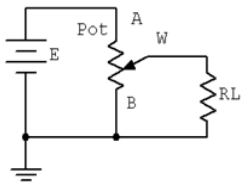


Figure 3.5.3.2

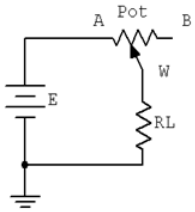


Figure 3.5.3.3

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3.5.4: Procedure

1. A typical potentiometer is shown in Figure 9.3.1. Using a 10 k pot, first rotate the knob fully counterclockwise and using the DMM, measure the resistance from terminal A to the wiper arm, W. Then measure the value from the wiper arm to terminal B. Record these values in Table 9.5.1. Add the two readings, placing the result in the final column.

2. Rotate the knob 1/4 turn clockwise and repeat the measurements of step 1. Repeat this process for the remaining knob positions in Table 9.5.1. Note that the results of the final column should all equal the nominal value of the potentiometer.

3. Construct the circuit of Figure 9.3.2 using E = 10 volts, a 10 k potentiometer and leave R_L open. Rotate the knob fully counter-clockwise and measure the voltage from the wiper to ground. Record this value in Table 9.5.2. Continue taking and recording voltages as the knob is rotated to the other four positions in Table 9.5.2.

4. Set R_L to 47 k and repeat step 3.

5. Set R_L to 4.7 k and repeat step 3.

6. Set R_L to 1 k and repeat step 3.

7. Using a linear grid, plot the voltages of Table 9.5.2 versus position. Note that there will be four curves created, one for each load, but place them on a single graph. Note how the variance of the load affects the linearity and control of the voltage.

8. Construct the circuit of Figure 9.3.3 using E = 10 volts, a 100 k potentiometer and R_L = 1 k. Rotate the knob fully counter-clockwise and measure the current through the load. Record this value in Table 9.5.3. Repeat this process for the remaining knob positions in Table 9.5.3.

9. Replace the load resistor with a 4.7 k and repeat step 8.

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3.5.5: Data Tables

Position	R_{AW}	R_{WB}	$R_{AW} + R_{WB}$
Fully CCW			
1/4			
1/2			
3/4			
Fully CW			

Table 3.5.5.1

Position	V_{WB} Open	V_{WB} 47k	V_{WB} 4.7k	V_{WB} 1k
Fully CCW				
1/4				
1/2				
3/4				
Fully CW				

Table 3.5.5.2

Position	I_L 1k	I_L 4.7k
Fully CCW		
1/4		
1/2		
3/4		
Fully CW		

Table 3.5.5.3

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3.5.6: Questions

1. In Table 9.5.1, does the total resistance always equal the nominal resistance of the potentiometer?

2. If the potentiometer used for Table 9.5.1 had a logarithmic taper, how would the values change?

3. In Table 9.5.2, is the load voltage always directly proportional to the knob position? Is the progression always linear?

4. Explain the variation of the four curves plotted in step 7.

5. In the final circuit, is the load current always proportional to the knob position? If the load was much smaller, say just a few hundred ohms, would the minimum and maximum currents be much different from those in Table 9.5.3?

6. How could the circuit of Figure 9.3.3 be modified so that the maximum current could be set to a value higher than that achieved by the supply and load resistor alone?

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CHAPTER OVERVIEW

4: Theorems and Analysis Methods

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  - 4.1.2: Equipment
  - 4.1.3: Schematics
  - 4.1.4: Procedure
  - 4.1.5: Data Tables
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SECTION OVERVIEW

4.1: Superposition Theorem

Objective

The objective of this exercise is to investigate the application of the superposition theorem to multiple DC source circuits in terms of both voltage and current measurements. Power calculations will also be examined.

4.1.1: Theory Overview

4.1.2: Equipment

4.1.3: Schematics

4.1.4: Procedure

4.1.5: Data Tables

4.1.6: Questions

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4.1.1: Theory Overview

The superposition theorem states that in a linear bilateral multi-source DC circuit, the current through or voltage across any particular element may be determined by considering the contribution of each source independently, with the remaining sources replaced with their internal resistance. The contributions are then summed, paying attention to polarities, to find the total value. Superposition cannot in general be applied to non-linear circuits or to non-linear functions such as power.

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4.1.2: Equipment

(1) Adjustable dual DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 4.7 kΩ

_____

(1) 6.8 kΩ

_____

(1) 10 kΩ

_____

(1) 22 kΩ

_____

(1) 33 kΩ

_____

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4.1.3: Schematics

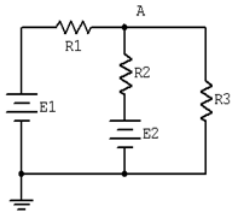


Figure 4.1.3.1

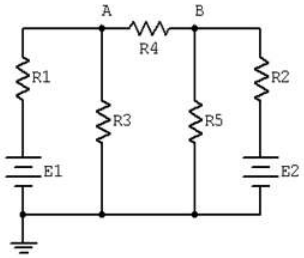


Figure 4.1.3.2

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4.1.4: Procedure

4.1.4.1 10.4.1: Voltage Application

1. Consider the dual supply circuit of Figure 10.3.1 using E1 = 10 volts, E2 = 15 volts, R1 = 4.7 k, R2 = 6.8 k and R3 = 10 k. To find the voltage from node A to ground, superposition may be used. Each source is considered by itself. First consider source E1 by assuming that E2 is replaced with its internal resistance (a short). Determine the voltage at node A using standard series-parallel techniques and record it in Table 10.5.1. Make sure to indicate the polarity. Repeat the process using E2 while shorting E1. Finally, sum these two voltages and record in Table 10.5.1.

2. To verify the superposition theorem, the process may be implemented directly by measuring the contributions. Build the circuit of Figure 10.3.1 with the values specified in step 1, however, replace E2 with a short. Do not simply place a shorting wire across source E2! This will overload the power supply.

3. Measure the voltage at node A and record in Table 10.5.1. Be sure to note the polarity.

4. Remove the shorting wire and insert source E2. Also, replace source E1 with a short. Measure the voltage at node A and record in Table 10.5.1. Be sure to note the polarity.

5. Remove the shorting wire and re-insert source E1. Both sources should now be in the circuit. Measure the voltage at node A and record in Table 10.5.1. Be sure to note the polarity. Determine and record the deviations between theory and experimental results.

4.1.4.2 10.4.2: Current and Power Application

6. Consider the dual supply circuit of Figure 10.3.2 using E1 = 10 volts, E2 = 15 volts, R1 = 4.7 k, R2 = 6.8 k, R3 = 10 k, R4 = 22 k and R5 = 33 k. To find the current through R4 flowing from node A to B, superposition may be used. Each source is again treated independently with the remaining sources replaced with their internal resistances. Calculate the current through R4 first considering E1 and then considering E2. Sum these results and record the three values in Table 10.5.2.

7. Assemble the circuit of Figure 10.3.2 using the values specified. Replace source E2 with a short and measure the current through R4. Be sure to note the direction of flow and record the result in Table 10.5.2.

8. Replace the short with source E2 and swap source E1 with a short. Measure the current through R4. Be sure to note the direction of flow and record the result in Table 10.5.2.

9. Remove the shorting wire and re-insert source E1. Both sources should now be in the circuit. Measure the current through R4 and record in Table 10.5.2. Be sure to note the direction. Determine and record the deviations between theory and experimental results.

10. Power is not a linear function as it is proportional to the square of either voltage or current. Consequently, superposition should not yield an accurate result when applied directly to power. Based on the measured currents in Table 10.5.2, calculate the power in R4 using E1-only and E2-only and record the values in Table 10.5.3. Adding these two powers yields the power as predicted by superposition. Determine this value and record it in Table 10.5.3. The true power in R4 may be determined from the total measured current flowing through it. Using the experimental current measured when both E1 and E2 were active (Table 10.5.2), determine the power in R4 and record it in Table 10.5.3.

4.1.4.3 10.4.3: Simulation

11. Build the circuit of Figure 10.3.2 in a simulator. Using the virtual DMM as an ammeter, determine the current through resistor R4 and compare it to the theoretical and measured values recorded in Table 10.5.2.

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4.1.5: Data Tables

Source	V_A Theory	V_A Experimental	Deviation
E1 Only			
E2 Only			
E1 and E2			

Table 4.1.5.1

Source	I_{R4} Theory	I_{R4} Experimental	Deviation
E1 Only			
E2 Only			
E1 and E2			

Table 4.1.5.2

Source	P_{R4}
E1 Only	
E2 Only	
E1 + E2	
E1 and E2	

Table 4.1.5.3

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4.1.6: Questions

1. Based on the results of Tables 10.5.1, 10.5.2 and 10.5.3, can superposition be applied successfully to voltage, current and power levels in a DC circuit?

2. If one of the sources in Figure 10.3.1 had been inserted with the opposite polarity, would there be a significant change in the resulting voltage at node A? Could both the magnitude and polarity change?

3. If both of the sources in Figure 10.3.1 had been inserted with the opposite polarity, would there be a significant change in the resulting voltage at node A? Could both the magnitude and polarity change?

4. Why is it important to note the polarities of the measured voltages and currents?

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SECTION OVERVIEW

4.2: Thévenin's Theorem

Objective

The objective of this exercise is to examine the use of Thévenin's Theorem to create simpler versions of DC circuits as an aide to analysis. Multiple methods of experimentally obtaining the Thévenin resistance will be explored.

4.2.1: Theory Overview

4.2.2: Equipment

4.2.3: Schematics

4.2.4: Procedure

4.2.5: Data Tables

4.2.6: Questions

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4.2.1: Theory Overview

Thévenin's Theorem for DC circuits states that any two port linear network may be replaced by a single voltage source with an appropriate internal resistance. The Thévenin equivalent will produce the same load current and voltage as the original circuit to any load. Consequently, if many different loads or subcircuits are under consideration, using a Thévenin equivalent may prove to be a quicker analysis route than "reinventing the wheel" each time.

The Thévenin voltage is found by determining the open circuit output voltage. The Thévenin resistance is found by replacing any DC sources with their internal resistances and determining the resulting combined resistance as seen from the two ports using standard series-parallel analysis techniques. In the laboratory, the Thévenin resistance may be found using an ohmmeter (again, replacing the sources with their internal resistances) or by using the matched load technique. The matched load technique involves replacing the load with a variable resistance and then adjusting it until the load voltage is precisely one half of the unloaded voltage. This would imply that the other half of the voltage must be dropped across the equivalent Thévenin resistance, and as the Thévenin circuit is a simple series loop then the two resistances must be equal as they have identical currents and voltages.

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4.2.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 2.2 kΩ

_____

(1) 3.3 kΩ

_____

(1) 4.7 kΩ

_____

(1) 6.8 kΩ

_____

(1) 8.2 kΩ

_____

(1) 10 k potentiometer or resistance decade box

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4.2.3: Schematics

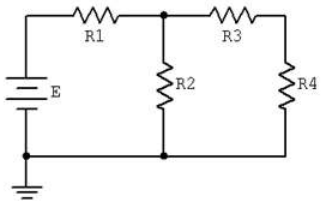


Figure 4.2.3.1

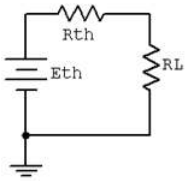


Figure 4.2.3.2

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4.2.4: Procedure

1. Consider the circuit of Figure 11.3.1 using E = 10 volts, R1 = 3.3 k, R2 = 6.8 k, R3 = 4.7 k and R4 (R_{Load}) = 8.2 k. This circuit may be analyzed using standard series-parallel techniques. Determine the voltage across the load, R4, and record it in Table 11.5.1. Repeat the process using 2.2 k for R4.

2. Build the circuit of Figure 11.3.1 using the values specified in step one, with R_{Load} = 8.2 k. Measure the load voltage and record it in Table 11.5.1. Repeat this with a 2.2 k load resistance. Determine and record the deviations. Do not deconstruct the circuit.

3. Determine the theoretical Thévenin voltage of the circuit of Figure 11.3.1 by finding the open circuit output voltage. That is, replace the load with an open and calculate the voltage produced between the two open terminals. Record this voltage in Table 11.5.2.

4. To calculate the theoretical Thévenin resistance, first remove the load and then replace the source with its internal resistance (ideally, a short). Finally, determine the combination series-parallel resistance as seen from the where the load used to be. Record this resistance in Table 11.5.2.

5. The experimental Thévenin voltage maybe determined by measuring the open circuit output voltage. Simply remove the load from the circuit of step one and then replace it with a voltmeter. Record this value in Table 11.5.2.

6. There are two methods to measure the experimental Thévenin resistance. For the first method, using the circuit of step one, replace the source with a short. Then replace the load with the ohmmeter. The Thévenin resistance may now be measured directly. Record this value in Table 11.5.2.

7. In powered circuits, ohmmeters are not effective while power is applied. An alternate method relies on measuring the effect of the load resistance. Return the voltage source to the circuit, replacing the short from step six. For the load, insert either the decade box or the potentiometer. Adjust this device until the load voltage is half of the open circuit voltage measured in step five and record in Table 11.5.2 under “Method 2”. At this point, the load and the Thévenin resistance form a simple series loop as seen in Figure 11.3.2. This means that they “see” the same current. If the load exhibits one half of the Thévenin voltage then the other half must be dropped across the Thévenin resistance, in other words $V_{RL} = V_{RTH}$. Consequently, the resistances have the same voltage and current, and therefore must have the same resistance according to Ohm’s law.

8. Consider the Thévenin equivalent of Figure 11.3.2 using the theoretical E_{TH} and R_{TH} from Table 11.5.2 along with 8.2 k for the load (RL). Calculate the load voltage and record it in Table 11.5.3. Repeat the process for a 2.2 k load.

9. Build the circuit of Figure 11.3.2 using the measured E_{TH} and R_{TH} from Table 11.5.2 along with 8.2 k for the load (RL). Measure the load voltage and record it in Table 11.5.3. Also determine and record the deviation.

10. Repeat step nine using a 2.2 k load.

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4.2.5: Data Tables

4.2.5.1 11.5.1: Original Circuit

R_4 (Load)	V_{Load} Theory	V_{Load} Experimental	Deviation
8.2 k			
2.2 k			

Table 4.2.5.1

4.2.5.2 11.5.2: Thévenized Circuit

	Theory	Experimental
E_{TH}		
R_{TH}		
R_{TH} Method 2	X	

Table 4.2.5.2

R_4 (Load)	V_{Load} Theory	V_{Load} Experimental	Deviation
8.2 k			
2.2 k			

Table 4.2.5.3

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4.2.6: Questions

1. Do the load voltages for the original and Thévenized circuits match for both loads? Is it logical that this could be extended to any arbitrary load resistance value?

2. Assuming several loads were under consideration, which is faster, analyzing each load with the original circuit of Figure 11.3.1 or analyzing each load with the Thévenin equivalent of Figure 11.3.2?

3. How would the Thévenin equivalent computations change if the original circuit contained more than one voltage source?

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SECTION OVERVIEW

4.3: Maximum Power Transfer

Objective

The objective of this exercise is to determine the conditions under which a load will produce maximum power. Further, the variance of load power and system efficiency will be examined graphically.

4.3.1: Theory Overview

4.3.2: Equipment

4.3.3: Schematics

4.3.4: Procedure

4.3.5: Data Tables

4.3.6: Questions

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4.3.1: Theory Overview

In order to achieve the maximum load power in a DC circuit, the load resistance must equal the driving resistance, that is, the internal resistance of the source. Any load resistance value above or below this will produce a smaller load power. System efficiency (η) is 50% at the maximum power case. This is because the load and the internal resistance form a basic series loop, and as they have the same value, they must exhibit equal currents and voltages, and hence equal powers. As the load increases in resistance beyond the maximizing value the load voltage will rise, however, the load current will drop by a greater amount yielding a lower load power. Although this is not the maximum load power, this will represent a larger percentage of total power produced, and thus a greater efficiency (the ratio of load power to total power).

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4.3.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) Resistance decade box

(1) 3.3 kΩ

_____

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4.3.3: Schematics

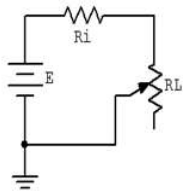


Figure 4.3.3.1

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4.3.4: Procedure

1. Consider the simple the series circuit of Figure 12.3.1 using E = 10 volts and Ri = 3.3 k. Ri forms a simple voltage divider with RL. The power in the load is VL^2 /RL and the total circuit power is E^2/(Ri+RL). The larger the value of RL, the greater the load voltage, however, this does not mean that very large values of RL will produce maximum load power due to the division by RL. That is, at some point VL^2 will grow more slowly than RL itself. This crossover point should occur when RL is equal to Ri. Further, note that as RL increases, total circuit power decreases due to increasing total resistance. This should lead to an increase in efficiency. An alternate way of looking at the efficiency question is to note that as RL increases, circuit current decreases. As power is directly proportional to the square of current, as RL increases the power in Ri must decrease leaving a larger percentage of total power going to RL.

2. Using RL = 30, compute the expected values for load voltage, load power, total power and efficiency, and record them in Table 12.5.1. Repeat for the remaining RL values in the Table. For the middle entry labeled Actual, insert the measured value of the 3.3 k used for Ri.

3. Build the circuit of Figure 12.3.1 using E = 10 volts and Ri = 3.3 k. Use the decade box for RL and set it to 30 ohms. Measure the load voltage and record it in Table 12.5.2. Calculate the load power, total power and efficiency, and record these values in Table 12.5.2. Repeat for the remaining resistor values in the table.

4. Create two plots of the load power versus the load resistance value using the data from the two tables, one for theoretical, one for experimental. For best results make sure that the horizontal axis (RL) uses a log scaling instead of linear.

5. Create two plots of the efficiency versus the load resistance value using the data from the two tables, one for theoretical, one for experimental. For best results make sure that the horizontal axis (RL) uses a log scaling instead of linear.

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4.3.5: Data Tables

R_L	V_L	P_L	P_T	η
30				
150				
500				
1 k				
2.5 k				
Actual=				
4 k				
10 k				
25 k				
70 k				
300 k				

Table 4.3.5.1

R_L	V_L	P_L	P_T	η
30				
150				
500				
1 k				
2.5 k				
Actual=				
4 k				
10 k				
25 k				
70 k				
300 k				

Table 4.3.5.2

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4.3.6: Questions

1. At what point does maximum load power occur?

2. At what point does maximum total power occur?

3. At what point does maximum efficiency occur?

4. Is it safe to assume that generation of maximum load power is always a desired goal? Why/why not?

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SECTION OVERVIEW

4.4: Nodal Analysis

Objective

The study of nodal analysis is the objective of this exercise, specifically its usage in multi-source DC circuits. Its application to finding circuit currents and voltages will be investigated.

4.4.1: Theory Overview

4.4.2: Equipment

4.4.3: Schematics

4.4.4: Procedure

4.4.5: Data Tables

4.4.6: Questions

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4.4.1: Theory Overview

Multi-source DC circuits may be analyzed using a node voltage technique. The process involves identifying all of the circuit nodes, a node being a point where various branch currents combine. A reference node, usually ground, is included. Kirchhoff's current law is then applied to each node. Consequently a set of simultaneous equations are created with an unknown voltage for each node with the exception of the reference. In other words, a circuit with a total of five nodes including the reference will yield four unknown node voltages and four equations. Once the node voltages are determined, various branch currents and component voltages may be derived.

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4.4.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 4.7 kΩ

_____

(1) 6.8 kΩ

_____

(1) 10 kΩ

_____

(1) 22 kΩ

_____

(1) 33 kΩ

_____

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4.4.3: Schematics

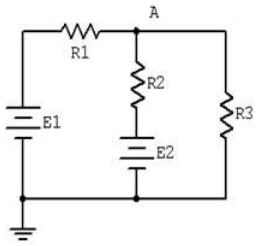


Figure 4.4.3.1

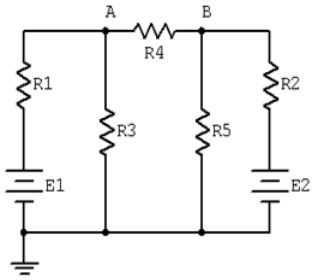


Figure 4.4.3.2

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4.4.4: Procedure

1. Consider the dual supply circuit of Figure 13.3.1 using E1 = 10 volts, E2 = 15 volts, R1 = 4.7 k, R2 = 6.8 k and R3 = 10 k. To find the voltage from node A to ground, nodal analysis may be applied. In this circuit note that there is only one node and therefore only one equation with one unknown is needed. Once this potential is found, all other circuit currents and voltages may be found by applying Ohm's law and/or KVL and KCL.

2. Write the node equation for the circuit of Figure 13.3.1 and solve for node voltage A. Also, determine the current through R3. Record these values in Table 13.5.1.

3. Construct the circuit of Figure 13.3.1 using the values specified in step one. Measure the voltage from node A to ground along with the current though R3. Record these values in Table 13.5.1. Also determine and record the deviations.

4. Consider the dual supply circuit of Figure 13.3.2 using E1 = 10 volts, E2 = 15 volts, R1 = 4.7 k, R2 = 6.8 k, R3 = 10 k, R4 = 22 k and R5 = 33 k. Applying nodal analysis to this circuit yields two equations with two unknowns, namely node voltages A and B. Again, once these potentials are found, any other circuit current or voltage may be determined by applying Ohm's law and/or KVL and KCL.

5. Write the node equations for the circuit of Figure 13.3.2 and solve for node voltage A, node voltage B and the potential from A to B. Also, determine the current through R4. Record these values in Table 13.5.2.

6. Construct the circuit of Figure 13.3.2 using the values specified in step four. Measure the voltages from node A to ground, node B to ground and from node A to B, along with the current though R4. Record these values in Table 13.5.2. Also determine and record the deviations.

4.4.4.1 13.4.1: Simulation

7. Build the circuit of Figure 13.3.2 in a simulator. Using the DC Operating Point simulation function, determine the voltages at nodes A and B, and compare these to the theoretical and measured values recorded in Table 13.5.2.

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4.4.5: Data Tables

Parameter	Theory	Experimental	Deviation
V_A			
I_{R3}			

Table 4.4.5.1

Parameter	Theory	Experimental	Deviation
V_A			
V_B			
V_AB			
I_{R4}			

Table 4.4.5.2

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4.4.6: Questions

1. Do the polarities of the sources in Figure 13.3.1 matter as to the resulting voltages? Will the magnitudes of the voltages be the same if one or both sources have an inverted polarity?

2. In both circuits of this exercise the negative terminals of the sources are connected to ground. Is this a requirement for nodal analysis? What would happen to the node voltages if the positions of E1 and R1 in Figure 13.3.1 were swapped?

3. The circuits of Figures 13.3.1 and 13.3.2 had been analyzed previously in the Superposition Theorem exercise. How do the results of this exercise compare to the earlier results? Should the resulting currents and voltages be identical? If not, what sort of things might affect the outcome?

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SECTION OVERVIEW

4.5: Mesh Analysis

Objective

The study of mesh analysis is the objective of this exercise, specifically its usage in multi-source DC circuits. Its application to finding circuit currents and voltages will be investigated.

4.5.1: Theory Overview

4.5.2: Equipment

4.5.3: Schematics

4.5.4: Procedure

4.5.5: Data Tables

4.5.6: Questions

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4.5.1: Theory Overview

Multi-source DC circuits may be analyzed using a mesh current technique. The process involves identifying a minimum number of small loops such that every component exists in at least one loop. Kirchhoff's voltage law is then applied to each loop. The loop currents are referred to as mesh currents as each current interlocks or meshes with the surrounding loop currents. As a result there will be a set of simultaneous equations created, an unknown mesh current for each loop. Once the mesh currents are determined, various branch currents and component voltages may be derived.

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4.5.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) 4.7 kΩ

_____

(1) 6.8 kΩ

_____

(1) 10 kΩ

_____

(1) 22 kΩ

_____

(1) 33 kΩ

_____

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4.5.3: Schematics

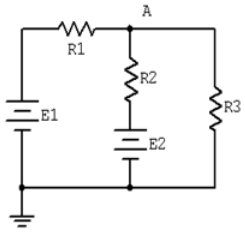


Figure 4.5.3.1

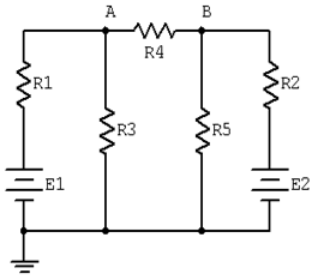


Figure 4.5.3.2

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4.5.4: Procedure

1. Consider the dual supply circuit of Figure 14.3.1 using E1 = 10 volts, E2 = 15 volts, R1 = 4.7 k, R2 = 6.8 k and R3 = 10 k. To find the voltage from node A to ground, mesh analysis may be used. This circuit may be described via two mesh currents, loop one formed with E1, R1, R2 and E2, and loop two formed with E2, R2 and R3. Note that these mesh currents are the currents flowing through R1 and R3 respectively.

2. Using KVL, write the loop expressions for these two loops and then solve to find the mesh currents. Note that the third branch current (that of R2) is the combination of the mesh currents and that the voltage at node A can be determined using the second mesh current and Ohm's law. Compute these values and record them in Table 14.5.1.

3. Build the circuit of Figure 14.3.1 using the values specified in step one. Measure the three branch currents and the voltage at node A and record in Table 14.5.1. Be sure to note the directions and polarities. Finally, determine and record the deviations in Table 14.5.1.

4. Consider the dual supply circuit of Figure 14.3.2 using E1 = 10 volts, E2 = 15 volts, R1 = 4.7 k, R2 = 6.8 k, R3 = 10 k, R4 = 22 k and R5 = 33 k. This circuit will require three loops to describe fully. This means that there will be three mesh currents in spite of the fact that there are five branch currents. The three mesh currents correspond to the currents through R1, R2, and R4.

5. Using KVL, write the loop expressions for these loops and then solve to find the mesh currents. Note that the voltages at nodes A and B can be determined using the mesh currents and Ohm's law. Compute these values and record them in Table 14.5.2.

6. Build the circuit of Figure 14.3.2 using the values specified in step four. Measure the three mesh currents and the voltages at node A, node B, and from node A to B, and record in Table 14.5.2. Be sure to note the directions and polarities. Finally, determine and record the deviations in Table 14.5.2.

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4.5.5: Data Tables

Parameter	Theory	Experimental	Deviation
I_{R1}			
I_{R2}			
I_{R3}			
V_A			

Table 4.5.5.1

Parameter	Theory	Experimental	Deviation
I_{R1}			
I_{R2}			
I_{R4}			
V_A			
V_B			
V_AB			

Table 4.5.5.2

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4.5.6: Questions

1. Do the polarities of the sources in Figure 14.3.1 matter as to the resulting currents? Will the magnitudes of the currents be the same if one or both sources have an inverted polarity?

2. In both circuits of this exercise the negative terminals of the sources are connected to ground. Is this a requirement for mesh analysis? What would happen to the mesh currents if the positions of E1 and R1 in Figure 14.3.1 were swapped?

3. The circuits of Figures 14.3.1 and 14.3.2 had been analyzed previously in the Superposition Theorem and Nodal Analysis exercises. How do the results of this exercise compare to the earlier results? Should the resulting currents and voltages be identical? If not, what sort of things might affect the outcome?

4. In general, compare and contrast the application of Superposition, Mesh and Nodal Analyses to multisource DC circuits. What are the advantages and disadvantages of each? Are some circuits better approached with a particular technique? Will each technique enable any particular current or voltage to be found or are there limitations?

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CHAPTER OVERVIEW

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SECTION OVERVIEW

5.1: The Oscilloscope

Objective

This exercise is of a particularly practical nature, namely, introducing the use of the oscilloscope. The various input scaling, coupling, and triggering settings are examined along with a few specialty features.

5.1.1: Theory Overview

5.1.2: Equipment

5.1.3: Components

5.1.4: Schematics and Diagrams

5.1.5: Procedure

5.1.6: Data Tables

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5.1.1: Theory Overview

The oscilloscope (or simply scope, for short) is arguably the single most useful piece of test equipment in an electronics laboratory. The primary purpose of the oscilloscope is to plot a voltage versus time although it can also be used to plot one voltage versus another voltage, and in some cases, to plot voltage versus frequency. Oscilloscopes are capable of measuring both AC and DC waveforms, and unlike typical DMMs, can measure AC waveforms of very high frequency (typically 100 MHz or more versus an upper limit of around 1 kHz for a general purpose DMM). It is also worth noting that a DMM will measure the RMS value of an AC sinusoidal voltage, not its peak value.

While the modern digital oscilloscope on the surface appears much like its analog ancestors, the internal circuitry is far more complicated and the instrument affords much greater flexibility in measurement. Modern digital oscilloscopes typically include measurement aides such as horizontal and vertical cursors or bars, as well as direct readouts of characteristics such as waveform amplitude and frequency. At a minimum, modern oscilloscopes offer two input measurement channels although four and eight channel instruments are increasing in popularity.

Unlike handheld DMMs, most oscilloscopes measure voltages with respect to ground, that is, the inputs are not floating and thus the black, or ground, lead is always connected to the circuit ground or common node. This is an extremely important point as failure to remember this may lead to the inadvertent short circuiting of components during measurement. The standard accepted method of measuring a non-ground referenced potential is to use two probes, one tied to each node of interest, and then setting the oscilloscope to subtract the two channels rather than display each separately. Note that this technique is not required if the oscilloscope has floating inputs (for example, in a handheld oscilloscope). Further, while it is possible to measure non-ground referenced signals by floating the oscilloscope itself through defeating the ground pin on the power cord, this is a safety violation and should not be done.

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5.1.2: Equipment

(1) DC power supply

model:_____ srn:_____

(1) AC function generator

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) Oscilloscope, Tektronix MDO 3000 series

model:_____ srn:_____

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5.1.3: Components

(1) 10 kΩ

actual:_____

(1) 33 kΩ

actual:_____

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5.1.4: Schematics and Diagrams

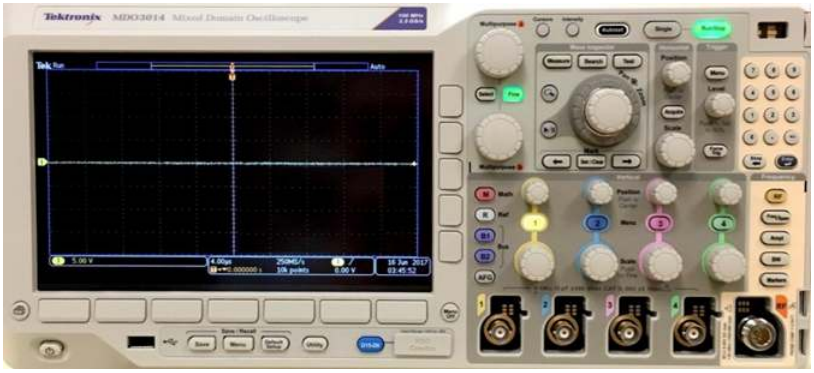


Figure 5.1.4.1

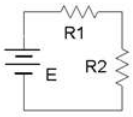


Figure 5.1.4.2

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5.1.5: Procedure

1. Figure 3.4.1 is a photo of the face of a Tektronix MDO 3000 series oscilloscope. Compare this to the bench oscilloscope and identify the following elements:

- Channel one through four BNC input connectors.
- RF input connector and settings section.
- Channel one through four select buttons.
- Horizontal Scale (i.e., Sensitivity) and Position knobs.
- Four Vertical Scale (i.e., Sensitivity) and Position knobs.
- Trigger Level knob.
- **Math** and **Measure** (in **Wave Inspector**) buttons.
- **Save** button (below display).
- **Autoset** button.
- **Menu Off** button.

2. Note the numerous buttons along the bottom and side of the display screen. These menu buttons are context-sensitive and their function will depend on the most recently selected button or knob. Menus may be removed from the display by pressing the **Menu Off** button (multiple times for nested menus). Power up the oscilloscope. Note that the main display is similar to a sheet of graph paper. Each square will have an appropriate scaling factor or weighting, for example, 1 volt per division vertically or 2 milliseconds per division horizontally. Waveform voltages and timings may be determined directly from the display by using these scales.

3. Select the channel one and two buttons (yellow and blue) and also press the **Autoset** button. (Autoset tries to create reasonable settings based on the input signal and is useful as a sort of “panic button”). There should now be two horizontal lines on the display, one yellow and one blue. These traces may be moved vertically on the display via the associated Position knobs. Also, a trace can be removed by deselecting the corresponding channel button. The Vertical and Horizontal Scale knobs behave in a similar fashion and do not include calibration markings. That is because the settings for these knobs show up on the main display. Adjust the Scale knobs and note how the corresponding values at the bottom of the display change. Voltages are in a 1/2/5 scale sequence while Time is in a 1/2/4 scale sequence.

4. When an input is selected, a menu will pop up allowing control over that input's basic settings. One of the more important fundamental settings on an oscilloscope channel is the **Input Coupling**. This is controlled via one of the bottom row buttons. There are two choices: **AC** allows only AC signals through thus blocking DC, and **DC** allows all signals through (it does not prevent AC).

5. Set the channel one Vertical Scale to 5 volts per division. Set the channel two Scale to 2 volts per division. Set the Time (Horizontal) Scale to 1 millisecond per division. Finally, set the input Coupling to DC for both input channels and align the blue and yellow display lines to the center line of the display via the Vertical Position knob (note that pushing the vertical Position knobs will automatically center the trace).

6. Build the circuit of Figure 3.4.2 using E = 10 V, R1 = 10 kΩ and R2 = 33kΩ. Connect a probe from the channel one input to the power supply (red or tip to the positive terminal, black clip to ground). Connect a second probe from channel two to R2 (again, red or tip to the high side of the resistor and the black clip to ground).

7. The yellow and blue lines should have deflected upward. Channel one should be raised two divisions (2 divisions at 5 volts per division yields the 10 volt source). Using this method, determine the voltage across R2 (remember, input two should have been set for 2 volts per division). Calculate the expected voltage across R2 using measured resistor values and compare the two in Table 3.6.1. Note that it is not possible to achieve extremely high precision using this method (e.g., four or more digits). Indeed, a DMM is often more useful for direct measurement of DC potentials. Double check the results using a DMM and the final column of Table 3.6.1.

8. Select AC Coupling for the two inputs. The flat DC lines should drop back to zero. This is because AC Coupling blocks DC. This will be useful for measuring the AC component of a combined AC/DC signal, such as might be seen in an audio amplifier. Set the input coupling for both channels back to DC.

9. Replace the DC power supply with the function generator. Set the function generator for a one volt peak sine wave at 1 kHz and apply it to the resistor network. The display should now show two small sine waves. Adjust the Vertical Scale settings for the two inputs so that the waves take up the majority of the display. If the display is very blurry with the sine waves appearing to jump about side to side, the Trigger Level may need to be adjusted. Also, adjust the Time Scale so that only one or two cycles of the wave may be seen. Using the Scale settings, determine the two voltages (following the method of step 7) as well as the waveform's period and compare them to the values expected via theory, recording the results in Tables 3.6.2 and 3.6.3. Also crosscheck the results using a DMM to measure the RMS voltages.

10. To find the voltage across R1, the channel two voltage (V_{R2}) may be subtracted from channel one (E source) via the **Math** function. Use the red button to select the **Math** function and create the appropriate expression from the menu (ch1 – ch2). This display shows up in red. To remove a waveform, press its button again. Remove the math waveform before proceeding to the next step.

11. One of the more useful aspects of the oscilloscope is the ability to show the actual waveshape. This may be used, for example, as a means of determining distortion in an amplifier. Change the waveshape on the function generator to a square wave, triangle, or other shape and note how the oscilloscope responds. Note that the oscilloscope will also show a DC component, if any, as the AC signal being offset or "riding on the DC". Adjust the function generator to add a DC offset to the signal and note how the oscilloscope display shifts. Return the function generator back to a sine wave and remove any DC offset.

12. It is often useful to take precise differential measurement on a waveform. For this, the bars or cursors are useful. Select the **Cursors** button toward the top of the oscilloscope. From the menu on the display, select **Vertical Bars**. Two vertical bars will appear on the display (it is possible that one or both could be positioned off the main display). They may be moved left and right via the Multipurpose knobs (next to the Cursors button). The **Select** button toggles between independent and tandem cursor movement. A read out of the bar values will appear in the upper portion of the display. They indicate the positions of the cursors, i.e., the location where they cross the waveform. Vertical Bars are very useful for obtaining time information as well as amplitudes at specific points along the wave. A similar function is the Horizontal Bars which are particularly useful for determining amplitudes. Try the Horizontal Bars by selecting them via the Cursors menu again (holding the **Cursors** button will bring up the menu).

13. For some waveform parameters, automatic readings are available. These are accessed via the **Measure** button. Press **Measure**, select **Add Measurement**, and page through the various options using the Multipurpose b knob. Select **Frequency**. Note that a small readout of the frequency will now appear on the display. Multiple measurements are possible simultaneously. Important: There are specific limits on the proper usage of these measurements. If the guidelines are not followed, erroneous values may result. Always perform an approximation via the Scale factor and divisions method even when using an automatic measurement!

14. Finally, a snap-shot of the screen may be saved for future work using the USB port and a USB memory stick via the **Save Menu** button. The pop up menu has options for saving the image as well as the trace data or setup info. **Select Save Screen Image** to save a bit mapped graphics file that can be used as is or processed further in a graphics program (for example, inverting the colors for printing). The .PNG format is recommended.

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5.1.6: Data Tables

V_{R2}	Scale (V/Div)	Number of Divisions	Voltage Scope	Voltage DMM
Oscilloscope				
Theory	X	X		

Table 5.1.6.1

	Scale (V/Div)	Number of Divisions	Voltage Peak	Voltage RMS
E Oscilloscope				
E Theory	X	X		
V_{R2} Oscilloscope				
V_{R2} Theory	X	X		

Table 5.1.6.2

	Scale (S/Div)	Number of Divisions	Period	Frequency
E Oscilloscope				
E Theory	X	X		

Table 5.1.6.3

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SECTION OVERVIEW

5.2: Capacitors and Inductors

Objective

The objective of this exercise is to become familiar with the basic behavior of capacitors and inductors. This includes determination of the equivalent of series and parallel combinations of each, the division of voltage among capacitors in series, and the steady state behavior of simple RLC circuits.

5.2.1: Theory Overview

5.2.2: Equipment

5.2.3: Schematics

5.2.4: Procedure

5.2.5: Data Tables

5.2.6: Questions

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5.2.1: Theory Overview

The inductor behaves identically to the resistor in terms of series and parallel combinations. That is, the equivalent of a series connection of inductors is simply the sum of the values. For a parallel connection of inductors either the product-sum rule or the "reciprocal of the sum of the reciprocals" rule may be used. Capacitors, in contrast, behave in an opposite manner. The equivalent of a parallel grouping of capacitors is simply the sum of the capacitances while a series connection must be treated with the product-sum or reciprocal rules.

For circuit analysis in the steady state case, inductors may be treated as shorts (or for more accuracy, as a small resistance known as the coil resistance, R_{coil}, which is dependent on the construction of the device) while capacitors may be treated as opens. If multiple capacitors are in series, the applied voltage will be split among them inversely to the capacitance. That is, the largest capacitors will drop the smallest voltages.

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5.2.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) RLC impedance meter

model:_____ srn:_____

(1) Digital multimeter

model:_____ srn:_____

(1) Electrostatic voltmeter (optional)

model:_____ srn:_____

(1) 4.7 kΩ

_____

(1) 10 kΩ

_____

(1) 100 nF

_____

(1) 220 nF

_____

(1) 1 mH

_____

(1) 10 mH

_____

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5.2.3: Schematics

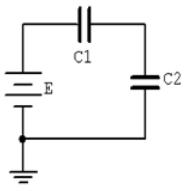


Figure 5.2.3.1

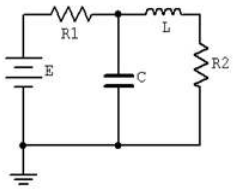


Figure 5.2.3.2

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5.2.4: Procedure

1. Using an RLC meter, measure the values of the two capacitors and two inductors and record them in Table 15.5.1. Also, measure the equivalent DC series resistance of the two inductors and record them in Table 15.5.1. Using these values, determine and record the theoretical series and parallel combinations specified in Table 15.5.2.

2. Connect the two capacitors in series and measure the total capacitance using the RLC meter. Record this value in Table 15.5.2. Repeat this process for the remaining combinations in Table 15.5.2. Also determine and record the deviations.

3. Consider the circuit of Figure 15.1 using E = 5 volts, C1 = 100 nF and C2 = 220 nF. Determine the voltage across each capacitor and record these values in Table 15.5.3.

4. Only perform this step if an electrostatic voltmeter is available for measurements as a typical DMM will give incorrect results due to loading effects. Build the circuit of Figure 15.1 using E = 5 volts, C1 = 100 nF and C2 = 220 nF. Measure the voltage across each capacitor and record these values in Table 15.5.3. Also determine and record the deviations.

5. Consider the circuit of Figure 15.2 using E = 10 volts, R1 = 4.7 k, R2 = 10 k, C = 100 nF and L = 1 mH. Determine the steady state voltage across each component and record these values in Table 15.5.4.

6. Build the circuit of Figure 15.2 using E = 10 volts, R1 = 4.7 k, R2 = 10 k, C = 100 nF and L = 1 mH. Energize the circuit. It will reach steady state in less than one second. Measure the steady state voltage across each component and record these values in Table 15.5.4. Also determine and record the deviations.

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5.2.5: Data Tables

5.2.5.1 15.5.1: Series and Parallel Combinations

Component	Experimental	R_{coil}
100 nF		X
220 nF		X
1 mH		
10 mH		

Table 5.2.5.1

Pairing	Theory	Experimental	Deviation
100 nF series 220 nF			
100 nF parallel 220 nF			
1 mH series 10 mH			
1 mH parallel 10 mH			

Table 5.2.5.2

5.2.5.2 15.5.2: Capacitive Series Circuit

Voltage	Theory	Experimental	Deviation
V_{C1}			
V_{C2}			

Table 5.2.5.3

5.2.5.3 15.5.3: Steady State RLC Circuit

Voltage	Theory	Experimental	Deviation
V_{R1}			
V_{R2}			
V_C			
V_L			

Table 5.2.5.4

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5.2.6: Questions

1. Does the value of R_{coil} appear to be correlated with the inductance value?
2. How do capacitors and inductors in series and in parallel compare with resistors?
3. In a series combination of capacitors, how does the voltage divide up?
4. For DC steady state analysis, what can be said about capacitors and inductors?
5. Does the value of R_{coil} seem to have much impact on the final circuit? Why/why not?

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SECTION OVERVIEW

5.3: Introduction to RL and RC Circuits

Objective

In this exercise, the DC steady state response of simple RL and RC circuits is examined. The transient behavior of RC circuits is also tested.

5.3.1: Theory Overview

5.3.2: Equipment

5.3.3: Components

5.3.4: Schematics

5.3.5: Procedure

5.3.6: Data Tables

5.3.7: Questions

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5.3.1: Theory Overview

The DC steady state response of RL and RC circuits are essential opposite of each other: that is, once steady state is reached, capacitors behave as open circuits while inductors behave as short circuits. In practicality, steady state is reached after five time constants. The time constant for an RC circuit is simply the effective capacitance times the effective resistance, $\tau = RC$. In the inductive case, the time constant is the effective inductance divided by the effective resistance, $\tau = L/R$.

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5.3.2: Equipment

(1) DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(1) Stop watch

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5.3.3: Components

(1) 1 μF

actual:_____

(1) 470 μF

actual:_____

(1) 10 mH

actual:_____

(1) 10 kΩ

actual:_____

(1) 47 kΩ

actual:_____

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5.3.4: Schematics

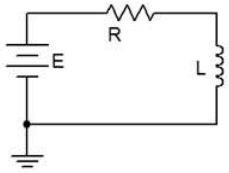


Figure 5.3.4.1

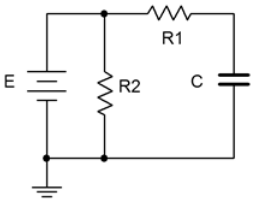


Figure 5.3.4.2

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5.3.5: Procedure

5.3.5.1 1.5.1: RL Circuit

1. Using Figure 1.4.1 with E = 10 V, R = 47 kΩ, and L = 10 mH, calculate the time constant and record it in Table 1.6.1. Also, calculate and record the expected steady state inductor voltage in Table 1.6.2.

2. Set the power supply to 10 V but do not hook it up to the remainder of the circuit. After connecting the resistor and inductor, connect the DMM across the inductor set to read DC voltage (20 volt scale).

3. Connect the power supply to the circuit. The circuit should reach steady state very quickly, in much less than one second. Record the experimental inductor voltage in Table 1.6.2. Also, compute and record the percent deviation between experimental and theory in Table 1.6.2.

5.3.5.2 1.5.2: RC Circuit

4. Using Figure 1.4.2 with E = 10 V, R1 = 47 kΩ, R2 = 10k and C = 1 μF, calculate the time constant and record it in Table 1.6.3. Also, calculate and record the expected steady state capacitor voltage in Table 1.6.4.

5. Set the power supply to 10 V but do not hook it up to the remainder of the circuit. After connecting the resistors and capacitor, connect the DMM across the capacitor set to read DC voltage (20 volt scale).

6. Connect the power supply to the circuit. The circuit should reach steady state quickly, in under one second. Record the experimental capacitor voltage in Table 1.6.4. Also, compute and record the percent deviation between experimental and theory in Table 1.6.4.

5.3.5.3 1.5.3: RC Circuit (long time constant)

7. Using Figure 1.4.2 with E = 10 V, R1 = 47k, R2 = 10 kΩ and C = 470 μF, calculate the time constants and record them in Table 1.6.5. Also, calculate and record the expected steady state capacitor voltage (charge phase) in Table 1.6.5.

8. Set the power supply to standby, and after waiting a moment for the capacitor to discharge, remove the capacitor and replace it with the 470 μF. Connect the DMM across the capacitor set to read DC voltage (20 volt scale).

9. Energize the circuit and record the capacitor voltage every 10 seconds as shown in Table 1.6.6. This is the charge phase.

10. Disconnect the power supply from the circuit and record the capacitor voltage every 10 seconds as shown in Table 1.6.7. This is the discharge phase.

11. Using the data from Tables 1.6.6 and 1.6.7, create two plots of capacitor voltage versus time and compare them to the theoretical plots found in the text.

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5.3.6: Data Tables

τ	

Table 5.3.6.1

V_L Theory	V_L Experimental	Deviation

Table 5.3.6.2

τ	

Table 5.3.6.3

V_C Theory	V_C Experimental	Deviation

Table 5.3.6.4

τ charge	
τ discharge	
V_C Theory	

Table 5.3.6.5

Time (sec)	Voltage
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	
110	
120	

Table 5.3.6.6

Time (sec)	Voltage
0	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	
110	
120	
130	
140	
150	

Table 5.3.6.7

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5.3.7: Questions

1. What is a reasonable approximation for an inductor at DC steady state?
2. What is a reasonable approximation for a capacitor at DC steady state?
3. How can a reasonable approximation for time-to-steady state of an RC circuit be computed?
4. In general, what sorts of shapes do the charge and discharge voltages of DC RC circuits follow?

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SECTION OVERVIEW

5.4: Capacitive Reactance

Objective

Capacitive reactance will be examined in this exercise. In particular, its relationship to capacitance and frequency will be investigated, including a plot of capacitive reactance versus frequency.

5.4.1: Theory Overview

5.4.2: Equipment

5.4.3: Components

5.4.4: Schematics

5.4.5: Procedure

5.4.6: Data Tables

5.4.7: Questions

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5.4.1: Theory Overview

The current – voltage characteristic of a capacitor is unlike that of typical resistors. While resistors show a constant resistance value over a wide range of frequencies, the equivalent ohmic value for a capacitor, known as capacitive reactance, is inversely proportional to frequency. The capacitive reactance may be computed via the formula:

$$X_C = -j\frac{1}{2\pi fC}$$

The magnitude of capacitive reactance may be determined experimentally by feeding a capacitor a known current, measuring the resulting voltage, and dividing the two, following Ohm's law. This process may be repeated a across a range of frequencies in order to obtain a plot of capacitive reactance versus frequency. An AC current source may be approximated by placing a large resistance in series with an AC voltage, the resistance being considerably larger than the maximum reactance expected.

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5.4.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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5.4.3: Components

(1) 1 μF

actual:_____

(1) 2.2 μF

actual:_____

(1) 10 kΩ

actual:_____

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5.4.4: Schematics

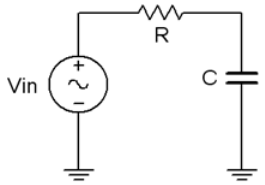


Figure 5.4.4.1

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5.4.5: Procedure

5.4.5.1 6.5.1: Current Source

1. Using Figure 6.4.1 with Vin = 10 V p-p and R = 10 kΩ, and assuming that the reactance of the capacitor is much smaller than 10k and can be ignored, determine the circulating current using measured component values and record in Table 6.6.1.

5.4.5.2 6.5.2: Measuring Reactance

2. Build the circuit of Figure 6.4.1 using R = 10 kΩ, and C = 1 μF. Place one probe across the generator and another across the capacitor. Set the generator to a 200 Hz sine wave and 10 V p-p. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings.

3. Calculate the theoretical value of Xc using the measured capacitor value and record in Table 6.6.2.

4. Record the peak-to-peak capacitor voltage and record in Table 6.6.2.

5. Using the source current from Table 6.6.1 and the measured capacitor voltage, determine the experimental reactance and record it in Table 6.6.2. Also compute and record the deviation.

6. Repeat steps three through five for the remaining frequencies of Table 6.6.2.

7. Replace the 1 μF capacitor with the 2.2 μF unit and repeat steps two through six, recording results in Table 6.6.3.

8. Using the data of Tables 6.6.2 and 6.6.3, create plots of capacitive reactance versus frequency.

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5.4.6: Data Tables

$i_{source(p-p)}$	

Table 5.4.6.1

Frequency	X_C Theory	$V_{C(p-p)}$ Exp	X_C Exp	% Dev
200				
400				
600				
800				
1.0 k				
1.2 k				
1.6 k				
2.0 k				

Table 5.4.6.2

Frequency	X_C Theory	$V_{C(p-p)}$ Exp	X_C Exp	% Dev
200				
400				
600				
800				
1.0 k				
1.2 k				
1.6 k				
2.0 k				

Table 5.4.6.3

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5.4.7: Questions

1. What is the relationship between capacitive reactance and frequency?

2. What is the relationship between capacitive reactance and capacitance?

3. If the experiment had been repeated with frequencies 10 times higher than those in Table 6.6.2, what would the resulting plots look like?

4. If the experiment had been repeated with frequencies 10 times lower than those in Table 6.6.2, what effect would that have on the experiment?

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SECTION OVERVIEW

5.5: Inductive Reactance

Objective

Inductive reactance will be examined in this exercise. In particular, its relationship to inductance and frequency will be investigated, including a plot of inductive reactance versus frequency.

5.5.1: Theory Overview

5.5.2: Equipment

5.5.3: Components

5.5.4: Schematics

5.5.5: Procedure

5.5.6: Data Tables

5.5.7: Questions

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5.5.1: Theory Overview

The current – voltage characteristic of an inductor is unlike that of typical resistors. While resistors show a constant resistance value over a wide range of frequencies, the equivalent ohmic value for an inductor, known as inductive reactance, is directly proportional to frequency. The inductive reactance may be computed via the formula:

$$X_L j2\pi fL$$

The magnitude of inductive reactance may be determined experimentally by feeding an inductor a known current, measuring the resulting voltage, and dividing the two, following Ohm's law. This process may be repeated a across a range of frequencies in order to obtain a plot of inductive reactance versus frequency. An AC current source may be approximated by placing a large resistance in series with an AC voltage, the resistance being considerably larger than the maximum reactance expected.

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5.5.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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5.5.3: Components

(1) 1 mH

actual:_____

(1) 10 mH

actual:_____

(1) 10 kΩ

actual:_____

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5.5.4: Schematics

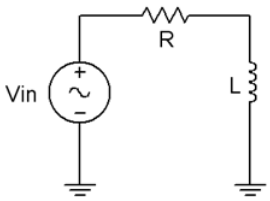


Figure 5.5.4.1

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5.5.5: Procedure

5.5.5.1 7.5.1: Current Source

1. Using Figure 7.4.1 with Vin=10 V p-p and R=10 kΩ, and assuming that the reactance of the inductor is much smaller than 10k and can be ignored, determine the circulating current using measured component values and record in Table 7.6.1. Also, measure the DC coil resistances of the inductors using an ohmmeter or DMM and record in Table 7.6.1.

5.5.5.2 7.5.2: Measuring Reactance

2. Build the circuit of Figure 7.4.1 using R=10 kΩ, and L=10 mH. Place one probe across the generator and another across the inductor. Set the generator to a 1000 Hz sine wave and 10 V p-p. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings.

3. Calculate the theoretical value of XL using the measured inductor value and record in Table 7.6.2.

4. Record the peak-to-peak inductor voltage and record in Table 7.6.2.

5. Using the source current from Table 7.6.1 and the measured inductor voltage, determine the experimental reactance and record it in Table 7.6.2. Also compute and record the deviation.

6. Repeat steps three through five for the remaining frequencies of Table 7.6.2.

7. Replace the 10 mH inductor with the 1 mH unit and repeat steps two through six, recording results in Table 7.6.3.

8. Using the data of Tables 7.6.2 and 7.6.3, create plots of inductive reactance versus frequency.

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5.5.6: Data Tables

$i_{source(p-p)}$	
R_{coil} of 10 mH	
R_{coil} of 1 mH	

Table 5.5.6.1

Frequency	X_L Theory	$V_{L(p-p)}$ Exp	X_L Exp	% Dev
1 k				
2 k				
3 k				
4 k				
5 k				
6 k				
8 k				
10 k				

Table 5.5.6.2

Frequency	X_L Theory	$V_{L(p-p)}$ Exp	X_L Exp	% Dev
10 k				
20 k				
30 k				
40 k				
50 k				
60 k				
80 k				
100 k				

Table 5.5.6.3

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5.5.7: Questions

1. What is the relationship between inductive reactance and frequency?

2. What is the relationship between inductive reactance and inductance?

3. If the 10 mH trial had been repeated with frequencies 10 times higher than those in Table 7.6.2, what effect would that have on the experiment?

4. Do the coil resistances have any effect on the plots?

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CHAPTER OVERVIEW

6: RLC Circuits and Filtering

6.1: Series RLC Circuits

6.1.1: Theory Overview

6.1.2: Equipment

6.1.3: Components

6.1.4: Schematics

6.1.5: Procedure

6.1.6: Data Tables

6.1.7: Questions

6.2: Parallel RLC Circuits

6.2.1: Theory Overview

6.2.2: Equipment

6.2.3: Components

6.2.4: Schematics

6.2.5: Procedure

6.2.6: Data Tables

6.2.7: Questions

6.3: Series-Parallel RLC Circuits

6.3.1: Theory Overview

6.3.2: Equipment

6.3.3: Components

6.3.4: Schematics

6.3.5: Procedure

6.3.6: Data Tables

6.3.7: Questions

6.4: Passive Crossover

6.4.1: Theory Overview

6.4.2: Equipment

6.4.3: Components

6.4.4: Schematics

6.4.5: Procedure

6.4.6: Data Tables

6.4.7: Questions

6.5: Series Resonance

6.5.1: Theory Overview

6.5.2: Equipment

6.5.3: Components

6.5.4: Schematics

6.5.5: Procedure

6.5.6: Data Tables

6.5.7: Questions
6.6: Parallel Resonance
6.6.1: Theory Overview
6.6.2: Equipment
6.6.3: Components
6.6.4: Schematics
6.6.5: Procedure
6.6.6: Data Tables
6.6.7: Questions

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SECTION OVERVIEW

6.1: Series RLC Circuits

Objective

This exercise examines the voltage and current relationships in series R, L, C networks. Of particular importance is the phase of the various components and how Kirchhoff's voltage law is extended for AC circuits. Both time domain and phasor plots of the voltages are generated.

6.1.1: Theory Overview

6.1.2: Equipment

6.1.3: Components

6.1.4: Schematics

6.1.5: Procedure

6.1.6: Data Tables

6.1.7: Questions

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6.1.1: Theory Overview

Each element has a unique phase response: for resistors, the voltage is always in phase with the current, for capacitors the voltage always lags the current by 90 degrees, and for inductors the voltage always leads the current by 90 degrees. Consequently, a series combination of R, L, and C components will yield a complex impedance with a phase angle between +90 and -90 degrees. Due to the phase response, Kirchhoff's voltage law must be computed using vector (phasor) sums rather than simply relying on the magnitudes. Indeed, all computations of this nature, such as a voltage divider, must be computed using vectors.

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6.1.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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6.1.3: Components

(1) 10 nF

actual:_____

(1) 10 mH

actual:_____

(1) 1 kΩ

actual:_____

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6.1.4: Schematics

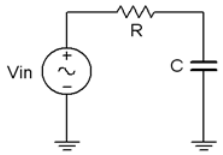


Figure 6.1.4.1

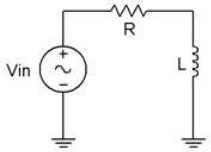


Figure 6.1.4.2

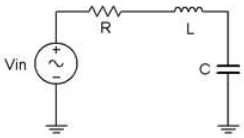


Figure 6.1.4.3

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6.1.5: Procedure

6.1.5.1 8.5.1: RC Circuit

1. Using Figure 8.4.1 with Vin = 2 V p-p sine at 10 kHz, R = 1 kΩ, and C = 10 nF, determine the theoretical capacitive reactance and circuit impedance, and record the results in Table 8.6.1 (the experimental portion of this table will be filled out in step 5). Using the voltage divider rule, compute the resistor and capacitor voltages and record them in Table 8.6.2.

2. Build the circuit of Figure 8.4.1 using R = 1 kΩ, and C = 10 nF. Place one probe across the generator and another across the capacitor. Set the generator to a 10 kHz sine wave and 2 V p-p. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings. Also, consider using Averaging for the acquisition mode, particularly to clean up signals derived using the Math function.

3. Measure the peak-to-peak voltage across the capacitor and record in Table 8.6.2. Along with the magnitude, be sure to record the time deviation between V_C and the input signal (from which the phase may be determined). Using the Math function, measure and record the voltage and time delay for the resistor $(V_{in}–V_C)$. Compute the phase angle and record these values in Table 8.6.2.

4. Take a snapshot of the oscilloscope displaying V_{in}, V_C, and V_R.

5. Compute the deviations between the theoretical and experimental values of Table 8.6.2 and record the results in the final columns of Table 8.6.2. Based on the experimental values, determine the experimental Z and X_C values via Ohm's law $(i = V_R/R, X_C = V_C/i, Z = V_{in}/i)$ and record back in Table 8.6.1 along with the deviations.

6. Create a phasor plot showing V_{in}, V_C, and V_R. Include both the time domain display from step 4 and the phasor plot with the technical report.

6.1.5.2 8.5.2: RL Circuit

7. Replace the capacitor with the 10 mH inductor (i.e. Figure 8.4.2), and repeat steps 1 through 6 in like manner, using Tables 8.6.3 and 8.6.4.

6.1.5.3 8.5.3: RLC Circuit

8. Using Figure 8.4.3 with both the 10 nF capacitor and 10 mH inductor, repeat steps 1 through 6 in similar manner, using Tables 8.6.5 and 8.6.6. Using a four channel oscilloscope: To obtain proper readings, place the first probe at the input, the second probe between the resistor and inductor, and the third probe between the inductor and capacitor. Probe three yields V_C. Using the Math function, probe two minus probe three yields V_L, and finally, probe one minus probe two yields V_R. Assigning Reference waveforms can be useful to see all of the signals together. Using a two channel oscilloscope: Unfortunately, it will be impossible to see the voltage of all three components simultaneously with the source voltage using a two channel oscilloscope. To obtain proper readings, place the first probe at the input and the second probe across the capacitor in order to see the phase and magnitude of V_C. Then, swap C and L (placing the second probe across the inductor) to see V_L, and finally, swap L and R (with the second probe across R) in order see V_R.

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6.1.6: Data Tables

6.1.6.1 8.6.1: RC Circuit

	Theory	Experimental	% Deviation
X_C			
Z Magnitude			
Z θ			

Table 6.1.6.1

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
V_C							
V_R							

Table 6.1.6.2

6.1.6.2 8.6.2: RL Circuit

	Theory	Experimental	% Deviation
X_L			
Z Magnitude			
Z θ			

Table 6.1.6.3

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
V_L							
V_R							

Table 6.1.6.4

6.1.6.3 8.6.3: RLC Circuit

	Theory	Experimental	% Deviation
X_C			
X_L			
Z Magnitude			
Z θ			

Table 6.1.6.5

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
V_C							
V_L							
V_R							

Table 6.1.6.6

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6.1.7: Questions

1. What is the phase relationship between R, L, and C components in a series AC circuit?

2. Based on measurements, does Kirchhoff's voltage law apply to the three tested circuits (show work)?

3. In general, how would the phasor diagram of Figure 8.6.1 change if the frequency was raised?

4. In general, how would the phasor diagram of Figure 8.6.2 change if the frequency was lowered?

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SECTION OVERVIEW

6.2: Parallel RLC Circuits

Objective

This exercise examines the voltage and current relationships in parallel R, L, C networks. Of particular importance is the phase of the various components and how Kirchhoff's current law is extended for AC circuits. Both time domain and phasor plots of the currents are generated. A technique to measure current using a current sense resistor will also be explored.

6.2.1: Theory Overview

6.2.2: Equipment

6.2.3: Components

6.2.4: Schematics

6.2.5: Procedure

6.2.6: Data Tables

6.2.7: Questions

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6.2.1: Theory Overview

Recall that for resistors, the voltage is always in phase with the current, for capacitors the voltage always lags the current by 90 degrees, and for inductors the voltage always leads the current by 90 degrees. Because each element has a unique phase response between +90 and -90 degrees, a parallel combination of R, L, and C components will yield a complex impedance with a phase angle between +90 and -90 degrees. Due to the phase response, Kirchhoff's current law must be computed using vector (phasor) sums rather than simply relying on the magnitudes. Indeed, all computations of this nature, such as a current divider, must be computed using vectors.

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6.2.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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6.2.3: Components

(1) 10 nF

actual:_____

(1) 10 mH

actual:_____

(1) 1 kΩ

actual:_____

(3) 10 Ω

actual:_____

actual:_____

actual:_____

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6.2.4: Schematics

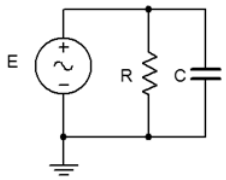


Figure 6.2.4.1

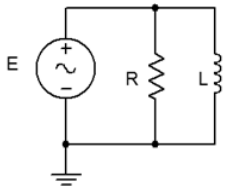


Figure 6.2.4.2

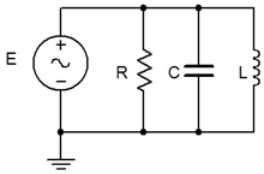


Figure 6.2.4.3

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6.2.5: Procedure

6.2.5.1 9.5.1: RC Circuit

1. Using Figure 9.4.1 with a 10 V p-p 10 kHz source, R = 1 kΩ, and C = 10 nF, determine the theoretical capacitive reactance and circuit impedance, and record the results in Table 9.6.1 (the experimental portion of this table will be filled out in step 6). Using the current divider rule, compute the resistor and capacitor currents and record them in Table 9.6.2.

2. Build the circuit of Figure 9.4.1 using R = 1 kΩ, and C = 10 nF. A common method to measure current using the oscilloscope is to place a small current sense resistor in line with the current of interest. If the resistor is much smaller than the surrounding reactances it will have a minimal effect on the current. Because the voltage and current of the resistor are always in phase with each other, the relative phase of the current in question must be the same as that of the sensing resistor's voltage. Each of the three circuit currents will be measured separately and with respect to the source in order to determine relative phase. To measure the total current, place a 10 Ω resistor between ground and the bottom connection of the parallel components. Set the generator to a 10 V p-p sine wave at 10 kHz. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings. Also, consider using waveform averaging, particularly to clean up signals derived via the Math function.

3. Place probe one across the generator and probe two across the sense resistor. Measure the voltage across the sense resistor, calculate the corresponding total current via Ohm's law and record in Table 9.6.2. Along with the magnitude, be sure to record the time deviation between the sense waveform and the input signal (from which the phase may be determined eventually).

4. Remove the main sense resistor and place one 10 Ω resistor between the capacitor and ground to serve as the capacitor current sense. Place a second 10 Ω resistor between the resistor and ground to sense the resistor current. Leave probe one at the generator and move probe two across the sense resistor in the resistor branch. Repeat the Ohm's law process to obtain its current, recording the magnitude and phase angle in Table 9.6.2. Finally, move probe two so that it is across the capacitor's sense resistor. Measure and record the appropriate values in Table 9.6.2. Note that if you are using a four channel oscilloscope, simultaneous input, resistor and capacitor measurements are possible.

5. Move probe one to the resistor's sense resistor and leave probe two at the capacitor's sense resistor. Save a picture of the oscilloscope displaying the voltage waveforms representing i_R, i_C and i_{in} (i.e., the Math waveform computed from $i_R + i_C$).

6. Compute the deviations between the theoretical and experimental values of Table 9.6.2 and record the results in the final columns of Table 9.6.2. Based on the experimental values, determine the experimental Z and X_C values via Ohm's law ($X_C = V_C/i_C, Z = V_{in}/i_{in}$) and record back in Table 9.6.1 along with the deviations.

7. Create a phasor plot showing i_{in}, i_C, and i_R. Include both the time domain display from step 4 and the phasor plot with the technical report.

6.2.5.2 9.5.2: RL Circuit

8. Replace the capacitor with the 10 mH inductor (i.e. Figure 9.4.2), and repeat steps 1 through 7 in like manner, using Tables 9.6.3 and 9.6.4.

6.2.5.3 9.5.3: RLC Circuit

9. Using Figure 9.4.3 with both the 10 nF capacitor and 10 mH inductor (and a third sense resistor), repeat steps 1 through 7 in like manner, using Tables 9.6.5 and 9.6.6. Note that it will not be possible to see all four waveforms simultaneously in step 5 if a two channel oscilloscope is being used. For a four channel oscilloscope, place a probe across each of the three sense resistors.

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6.2.6: Data Tables

6.2.6.1 9.6.1: RC Circuit

	Theory	Experimental	% Deviation
X_C			
Z Magnitude			
Z θ			

Table 6.2.6.1

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
i_C							
i_R							
i_{in}							

Table 6.2.6.2

6.2.6.2 9.6.2: RL Circuit

	Theory	Experimental	% Deviation
X_L			
Z Magnitude			
Z θ			

Table 6.2.6.3

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
i_L							
i_R							
i_{in}							

Table 6.2.6.4

6.2.6.3 9.6.3: RLC Circuit

	Theory	Experimental	% Deviation
X_C			
X_L			
Z Magnitude			
Z θ			

Table 6.2.6.5

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
i_C							
i_L							
i_R							
i_{in}							

Table 6.2.6.6

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6.2.7: Questions

1. What is the phase relationship between R, L, and C components in a parallel AC circuit?

2. Based on measurements, does Kirchhoff's current law apply to the three tested circuits (show work)?

3. In general, how would the phasor diagram of Figure 9.6.1 change if the frequency was raised?

4. In general, how would the phasor diagram of Figure 9.6.2 change if the frequency was lowered?

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SECTION OVERVIEW

6.3: Series-Parallel RLC Circuits

Objective

This exercise examines the voltage and current relationships in series-parallel R, L, C networks. Often series-parallel circuits may be analyzed along the lines of the simpler series-only or parallel-only circuits, but where each “element” may comprise a complex impedance rather than a singular R, L, or C component. Both Kirchhoff’s current law and Kirchhoff’s voltage law may be applied to these circuits. In this exercise, both time domain and phasor plots of the voltages and currents are generated.

6.3.1: Theory Overview

6.3.2: Equipment

6.3.3: Components

6.3.4: Schematics

6.3.5: Procedure

6.3.6: Data Tables

6.3.7: Questions

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6.3.1: Theory Overview

Many complex R, L, C networks may be analyzed by reducing them to simpler series or parallel circuits, perhaps through an iterative process in more involved instances. In this analysis each series or parallel element is in fact a complex impedance made up of a series or parallel combination of other components and thus producing a phase angle between +90 and -90 degrees. Consequently, the simple “all right angles” phasor diagrams found for basic series and parallel circuits may be replaced with more general phasor diagrams with non-right angles. In spite of this, both Kirchhoff’s current law and Kirchhoff’s voltage law must still be satisfied for the entire circuit, as well as any sub-circuits or branches.

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6.3.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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6.3.3: Components

(1) 10 nF actual:_____

(1) 10 mH actual:_____

(1) 1 kΩ actual:_____

(2) 10 Ω actual:_____

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6.3.4: Schematics

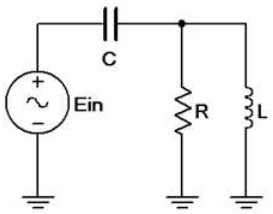


Figure 6.3.4.1

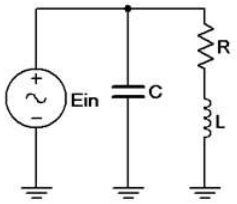


Figure 6.3.4.2

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6.3.5: Procedure

6.3.5.1 10.5.1: Circuit 1

1. Using Figure 10.4.1 with a 10 kHz sine wave at 10 V p-p source, R = 1 kΩ, L = 10 mH, and C = 10 nF, determine the theoretical inductive and capacitive reactances, parallel branch reactance and total circuit impedance, and record the results in Table 10.6.1 (the experimental portion of this table will be filled out in step 5). Using Ohm's law and the voltage divider rule compute the capacitor and inductor-resistor voltages along with the input current and record them in Table 10.6.2.

2. Build the circuit of Figure 10.4.1 using R = 1 kΩ, L = 10 mH, and C = 10 nF. Set the generator to a 10 kHz sine wave and 10 V p-p. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings.

3. Place probe one across the generator and probe two across the parallel inductor-resistor branch. Using the Math function, the capacitor voltage may be found by subtracting the voltage of probe two from that of probe one. Also, the input current may be found by dividing the capacitor's voltage by its reactance. Measure the parallel branch voltage and capacitor voltage, both magnitude and phase, and record in Table 10.6.2. Compute the input current and record in Table 10.6.2.

4. Take a picture of the three voltage waveforms.

5. Compute the deviations between the theoretical and experimental values of Table 10.6.2 and record the results in the final columns of Table 10.6.2. Based on the experimental values, determine the experimental total Z and parallel branch Z values via Ohm's law (e.g., $Z_T = V_{in}/i_{in}$) and record back in Table 10.6.1 along with the deviations.

6. Create a phasor plot showing V_{in}, V_{LR}, and V_C. Include both the time domain display from step 4 and the phasor plot with the technical report.

6.3.5.2 10.5.2: Circuit 2

7. Using Figure 10.4.2 with a 10k Hz sine wave at 10 V p-p, R = 1 kΩ, L = 10 mH, and C = 10 nF, determine the theoretical inductive and capacitive reactances, series branch impedance and total circuit impedance, and record the results in Table 10.6.3. Using Ohm's law compute the capacitor and inductor-resistor currents along with the input current and record them in Table 10.6.4.

8. Build the circuit of Figure 10.4.2 using R = 1 kΩ, L = 10 mH, and C = 10 nF. Insert a 10 Ω current sense resistor at the bottom of the LR leg and another at the bottom of the capacitor leg. Set the generator to a 10 kHz sine wave and 10 V p-p. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings.

9. Place probe one across the generator and probe two across the inductor-resistor branch sense resistor. The inductor-resistor current may be found by dividing the probe two voltage by the sense resistor. The capacitor current is found in a similar manner using its current sense resistor (use probe three if available, otherwise perform this twice using probe two). Record both magnitude and phase of the two currents in Table 10.6.4.

10. Take a picture of the V_{in} and i_{LR} sense waveforms and also of the V_{in} and i_C sense waveforms (one combined picture if using three probes, otherwise two separate pictures).

11. To measure the input current, remove the two sense resistors and place one of them so that it is between ground and the bottom junction of the resistor and capacitor. Move probe two to this sense resistor and measure the voltage. From this, compute the total current and record both magnitude and phase in Table 10.6.4.

12. Take a picture of the V_{in} and i_{in} sense waveforms.

13. Compute the deviations between the theoretical and experimental values of Table 10.6.4 and record the results in the final columns of Table 10.6.4. Based on the experimental values, determine the experimental total Z and series branch Z values and record back in Table 10.6.3 along with the deviations.

14. Create a phasor plot showing i_{in}, i_{LR}, and i_C. Include both the time domain displays from steps 10 & 12 and the phasor plot with the technical report.

6.3.5.3 10.5.3: Computer Simulation

15. Build the circuit of Figure 10.4.1 in a simulator. Using Transient Analysis, determine the voltage across the inductor and compare the magnitude and phase to the theoretical and measured values recorded in Table 10.6.2.

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6.3.6: Data Tables

6.3.6.1 10.6.1: Circuit 1

	Theory	Experimental	% Deviation
X_C		n/a	n/a
X_L		n/a	n/a
$R\|\|X_L$			
Z_T Magnitude			
Z_T θ			

Table 6.3.6.1

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
V_{LR}							
V_C							
i_{in}							

Table 6.3.6.2

6.3.6.2 10.6.2: Circuit 2

	Theory	Experimental	% Deviation
X_C		n/a	n/a
X_L		n/a	n/a
$R + X_L$			
Z_T Magnitude			
Z_T θ			

Table 6.3.6.3

	Theory Mag	Theory θ	Exp Mag	Exp Delay	Exp θ	% Dev Mag	% Dev θ
i_{LR}							
i_C							
i_{in}							

Table 6.3.6.4

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6.3.7: Questions

1. Is the phase relationship between circuit voltages or currents in a series-parallel AC circuit necessarily a right-angle relationship?

2. Based on measurements, do KVL and KCL apply to the tested circuits (show work)?

3. In general, how would the phasor diagram of Figure 10.6.1 change if the frequency was raised?

4. In general, how would the phasor diagram of Figure 10.6.2 change if the frequency was lowered?

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SECTION OVERVIEW

6.4: Passive Crossover

Objective

The frequency response of a simple two-way LC passive crossover is investigated. One output should attenuate signals above the crossover frequency while the other output should attenuate signals below the crossover frequency.

6.4.1: Theory Overview

6.4.2: Equipment

6.4.3: Components

6.4.4: Schematics

6.4.5: Procedure

6.4.6: Data Tables

6.4.7: Questions

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6.4.1: Theory Overview

In order to span the range of audible tones with accuracy, low distortion, and reasonable volume levels, loudspeaker systems are typically comprised of two or more transducers, each designed to cover only a portion of the frequency spectrum. As the spectrum is broken up into multiple segments, a circuit is needed to “steer” the proper signals to the appropriate transducers. Failure to do so may result in distortion or damage to the transducers. As inductors and capacitors exhibit a reactance that is a function of frequency, they are ideal candidates for this job. In this exercise, a simple two-way crossover is examined. It has one output for the high frequency transducer (tweeter) and for the low frequency transducer (woofer). In order to reduce the size of the components in this exercise, the impedance has been scaled upward by a factor of nearly 100. In place of the transducers, two resistive loads are used. This has the added advantage of not producing any sound in the lab! While real-world crossovers tend to be more complex than the one in this exercise, it will suffice to show the basic operation.

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6.4.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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6.4.3: Components

(1) 250 nF

actual:_____

(1) 100 mH

actual:_____

(2) 620 Ω

actual:_____

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6.4.4: Schematics

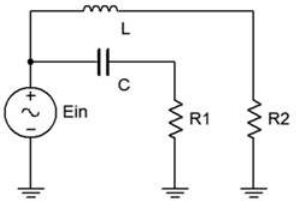


Figure 6.4.4.1

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6.4.5: Procedure

1. The circuit of Figure 11.4.1 can be thought of as a pair of frequency dependent voltage dividers. X_L increases with frequency, thus attenuating high frequency signals reaching R2. Similarly, X_C increases with a decrease in frequency, thus attenuating low frequency signals reaching R1. (R2 takes the place of the woofer while R1 takes the place of the tweeter). The crossover frequency is the frequency where R1 = X_C and R2 = X_L (normally the same frequency for both). Using C = 250 nF, L = 100 mH, and R1 = R2 = 620 Ω, determine the crossover frequencies and record in Table 11.6.1.

2. Using the voltage divider rule and E_{in} = 2 V p-p, determine and record the theoretical voltage at output one (R1) for each frequency listed in Table 11.6.2. Be sure to include both magnitude and phase.

3. Build the circuit of Figure 11.4.1 using R1 = R2 = 620 Ω, L = 100 mH, and C = 250 nF. Place one probe across the generator and another across output one (R1). Set the generator to a 2 V p-p sine wave at 50 Hz. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings.

4. Measure and magnitude and phase shift of the output with respect to the input and record in Table 11.6.2. Repeat the measurements for the remaining frequencies in the table.

5. Repeat Steps two through four using the second output (R2) and Table 11.6.3.

6. On a single graph plot the magnitude response of both outputs with respect to frequency. On a separate graph plot the phase response of both outputs with respect to frequency.

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6.4.6: Data Tables

$f_{tweeter}$	
f_{woofer}	

Table 6.4.6.1

6.4.6.1 11.6.1: Output One

Frequency	$V1$ Mag Theory	$V1$ θ Theory	$V1$ Mag Exp	$V1$ θ Exp
50				
70				
100				
200				
500				
1k				
2k				
5k				
10k				
15k				
20k				

Table 6.4.6.2

6.4.6.2 11.6.2: Output Two

Frequency	$V2$ Mag Theory	$V2$ θ Theory	$V2$ Mag Exp	$V2$ θ Exp
50				
70				
100				
200				
500				
1k				
2k				
5k				
10k				
15k				
20k				

Table 6.4.6.3

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6.4.7: Questions

1. Are the responses of the two outputs symmetrical? Do they need to be?

2. What is the maximum attenuation at the frequency extremes for the two outputs?

3. How might the attenuation be increased?

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SECTION OVERVIEW

6.5: Series Resonance

Objective

This exercise investigates the voltage relationships in a series resonant circuit. Of primary importance are the establishment of the resonant frequency and the quality factor, or Q, of the circuit with relation to the values of the R, L, and C components.

6.5.1: Theory Overview

6.5.2: Equipment

6.5.3: Components

6.5.4: Schematics

6.5.5: Procedure

6.5.6: Data Tables

6.5.7: Questions

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6.5.1: Theory Overview

A series resonant circuit consists of a resistor, a capacitor, and an inductor in a simple loop. At some frequency the capacitive and inductive reactances will be of the same magnitude, and as they are 180 degrees in opposition, they effectively nullify each other. This leaves the circuit purely resistive, the source “seeing” only the resistive element. Consequently, the current will be at a maximum at the resonant frequency. At any higher or lower frequency, a net reactance (the difference between X_L and X_C) must be added to the resistor value, producing a higher impedance and thus, a lower current. As this is a simple series loop, the resistor’s voltage will be proportional to the current. Consequently, the resistor voltage should be a maximum at the resonant frequency and decrease as the frequency is either increased or decreased. At resonance, the resistor value sets the maximal current and consequently has a major effect on the voltages developed across the capacitor and inductor as well as the “tightness” of the voltage versus frequency curve: The smaller the resistance, the tighter the curve and the higher the voltage seen across the capacitor and inductor. The Q of the circuit can be defined as the ratio of the resonant reactance to the circuit resistance, Q = X/R, which also corresponds to the ratio of the resonant frequency to the circuit bandwidth, Q = F_0/BW.

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6.5.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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6.5.3: Components

(1) 10 nF actual:_____

(1) 10 mH actual:_____

(1) 47 Ω actual:_____

(1) 470 Ω actual:_____

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6.5.4: Schematics

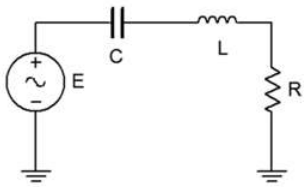


Figure 6.5.4.1

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6.5.5: Procedure

6.5.5.1 15.5.1: Low Q Circuit

1. Using Figure 15.4.1 with R = 470 Ω, L = 10 mH, and C = 10 nF, determine the theoretical resonance frequency and Q, and record the results in Table 15.6.1. Based on these values determine the upper and lower frequencies defining the bandwidth, f_1 and f_2, and record them in Table 15.6.1.

2. Build the circuit of Figure 15.4.1 using R = 470 Ω, L = 10 mH and C = 10 nF. Place a probe across the resistor. Set the output of the generator to a 1 V p-p sine wave. Set the frequency to the theoretical resonance frequency of Table 15.6.1. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings.

3. Adjust the frequency in small amounts, up and down, until the maximum voltage is found. This is the experimental resonance frequency. Record it in Table 15.6.1. Note the amplitude (it should be approximately equal to the source voltage of 1 V p-p). Sweep the frequency above and below the resonance frequency until the experimental f_1 and f_2 are found. These will occur at a voltage amplitude of approximately 0.707 times the resonant voltage (i.e., the half-power points). Record these frequencies in Table 15.6.1. Also, determine and record the experimental Q based on the experimental f_0, f_1, and f_2.

4. Transcribe the experimental frequencies of Table 15.6.1 to the top three entries of Table 15.6.2. For all of the frequencies in Table 15.6.2, measure and record the voltage across the resistor. Also measure and record the inductor and capacitor voltages. Note that the inductor and capacitor will have to be swapped with the resistor position in order to maintain proper ground reference with the oscilloscope.

5. Based on the data from Table 15.6.2, plot V_R, V_C, and V_L as a function of frequency.

6. Change R to 47Ω and repeat steps 1 through 5 but using Tables 15.6.3 and 15.6.4 for high Q.

6.5.5.2 15.5.2: Computer Simulation

7. Build the circuit of Figure 15.4.1 in a simulator. Using AC Analysis, plot the voltage across the resistor from 1 kHz to 100 kHz for both the high and low Q cases and compare them to the plots derived from Tables 15.6.2 and 15.6.4. Be sure to include the 50 Ω source resistance and coil resistance in the simulation.

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6.5.6: Data Tables

6.5.6.1 15.6.1: Low Q Circuit

	Theory	Experimental	% Deviation
f_o			
Q			
f_1			
f_2			

Table 6.5.6.1

Frequency	V_R	V_C	V_L
f_0=			
f_1=			
f_2=			
1 kHz			
5 kHz			
8 kHz			
12 kHz			
20 kHz			
30 kHz			
50 kHz			
100 kHz			

Table 6.5.6.2

6.5.6.2 15.6.2: High Q Circuit

	Theory	Experimental	% Deviation
f_o			
Q			
f_1			
f_2			

Table 6.5.6.3

Frequency	V_R	V_C	V_L
f_0=			
f_1=			
f_2=			
1 kHz			
5 kHz			
8 kHz			
12 kHz			
20 kHz			
30 kHz			
50 kHz			
100 kHz			

Table 6.5.6.4

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6.5.7: Questions

1. What is the effect of changing resistance on Q?

2. Are the V_C and V_L curves the same as the V_R curves? If not, why?

3. In practical terms, what sets the limit on how high Q may be?

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SECTION OVERVIEW

6.6: Parallel Resonance

Objective

This exercise investigates the voltage relationships in a parallel resonant circuit. Of primary importance are the establishment of the resonant frequency and the quality factor, or Q, of the circuit with relation to the values of the R, L, and C components.

6.6.1: Theory Overview

6.6.2: Equipment

6.6.3: Components

6.6.4: Schematics

6.6.5: Procedure

6.6.6: Data Tables

6.6.7: Questions

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6.6.1: Theory Overview

A parallel resonant circuit consists of a resistor, a capacitor, and an inductor in parallel, typically driven by a current source. At some frequency the capacitive and inductive reactances will be of the same magnitude, and as they are 180 degrees in opposition, they effectively nullify each other. This leaves the circuit purely resistive, the source “seeing” only the resistive element. At any lower or higher frequency the inductive or capacitive reactance will shunt the resistance. The result is a maximum impedance magnitude at resonance, and thus, a maximum voltage. Any resistance value in series (such as the inductor’s coil resistance) should be transformed into a parallel resistance in order to gauge its effect on the system voltage. The combined parallel resistance sets the Q of the circuit and can be defined as the ratio of the combined resistance to the resonant reactance, Q = R/X, which also corresponds to the ratio of the resonant frequency to the circuit bandwidth, Q = f_0/BW.

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6.6.2: Equipment

(1) AC function generator

model:_____ srn:_____

(1) Oscilloscope

model:_____ srn:_____

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6.6.3: Components

(1) 10 nF

actual:_____

(1) 10 mH

actual:_____

(1) 2.2 kΩ

actual:_____

(1) 10 kΩ

actual:_____

(1) 100 kΩ

actual:_____

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6.6.4: Schematics

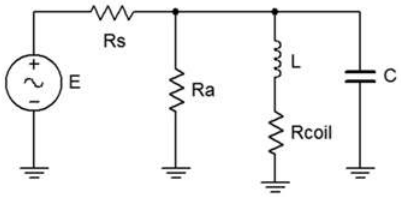


Figure 6.6.4.1

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6.6.5: Procedure

1. Using Figure 16.4.1 with Rs = 100 kΩ, Ra = 2.2 kΩ, L = 10 mH, Rcoil = 7 Ω and C = 10 nF, determine the theoretical resonance frequency and Q, and record the results in Table 16.6.1. Based on these values determine the upper and lower frequencies defining the bandwidth, f_1 and f_2, and record them in Table 16.6.1 also.

2. Build the circuit of Figure 16.4.1 using Rs = 100 kΩ, Ra = 2.2 kΩ, L = 10 mH and C = 10 nF. Set the output of the generator to a 10 V p-p sine wave at the theoretical resonant frequency. The large value of Rs associated with the voltage source will make it appear as a current source equal to approximately 100 μA p-p, assuming the parallel branch impedance is much less than Rs. Place a probe across the parallel branch. Set the frequency to the theoretical resonance frequency of Table 16.6.1. Make sure that the Bandwidth Limit of the oscilloscope is engaged for both channels. This will reduce the signal noise and make for more accurate readings.

3. Adjust the frequency in small amounts, up and down, until the maximum voltage is found. This is the experimental resonant frequency. Record it in Table 16.6.1. Note the amplitude. Sweep the frequency above and below the resonance frequency until the experimental f_1 and f_2 are found. These will occur at a voltage amplitude of approximately 0.707 times the resonant voltage (i.e., the half-power points). Record these frequencies in Table 16.6.1. Also, determine and record the experimental Q based on the experimental f_0, f_1, and f_2.

4. Transcribe the experimental frequencies of Table 16.6.1 to the top three entries of Table 16.6.2. For all of the frequencies in Table 16.6.2, measure and record the voltage across the parallel branch.

5. Based on the data from Table 16.6.2, plot the parallel branch voltage as a function of frequency.

6. For high Q, change Ra to 10 kΩ and repeat steps 1 through 5 but using Tables 16.6.3 and 16.6.4.

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6.6.6: Data Tables

6.6.6.1 16.6.1: Low Q Circuit

	Theory	Experimental	% Deviation
f_o			
Q			
f_1			
f_2			

Table 6.6.6.1

Frequency	$V_{Parallel}$
f_0=	
f_1=	
f_2=	
1 kHz	
5 kHz	
8 kHz	
12 kHz	
20 kHz	
30 kHz	
50 kHz	
100 kHz	

Table 6.6.6.2

6.6.6.2 16.6.2: High Q Circuit

	Theory	Experimental	% Deviation
f_o			
Q			
f_1			
f_2			

Table 6.6.6.3

Frequency	$V_{parallel}$
f_0=	
f_1=	
f_2=	
1 kHz	
5 kHz	
8 kHz	
12 kHz	
20 kHz	
30 kHz	
50 kHz	
100 kHz	

Table 6.6.6.4

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6.6.7: Questions

1. What is the effect of changing resistance on Q?

2. Are f_1 and f_2 spaced symmetrically around f_0?

3. In practical terms, what sets the limit on how high Q may be?

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CHAPTER OVERVIEW

7: Diodes

7.1: Diode Curves
- 7.1.1: Theory Overview
- 7.1.2: Equipment
- 7.1.3: Schematics
- 7.1.4: Procedure
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SECTION OVERVIEW

7.1: Diode Curves

Objective

The objective of this exercise is to examine the operation of the basic switching diode and to plot its characteristic curve. Basic DC circuit operation will also be examined.

7.1.1: Theory Overview

7.1.2: Equipment

7.1.3: Schematics

7.1.4: Procedure

7.1.5: Data Tables

7.1.6: Questions

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7.1.1: Theory Overview

The basic diode is an asymmetric non-linear device. That is, its current-voltage characteristic is not a straight line and it is sensitive to the polarity of an applied voltage or current. When placed in forward bias (i.e. positive polarity from anode to cathode), the diode will behave much like a shorted switch and allow current flow. When reversed biased the diode will behave much like an open switch, allowing little current flow. Unlike a switch, a silicon diode will exhibit an approximate 0.7 volt drop when forward biased. The precise voltage value will depend on the semiconductor material used. This volt drop is sometimes referred to as the knee voltage as the resulting I-V curve looks something like a bent knee.

The effective instantaneous resistance of the diode above the turn-on threshold is very small, perhaps a few ohms or less, and is often ignored. Analysis of diode circuits typically proceeds by determining if the diode is forward or reversed biased, substituting the appropriate approximation for the device, and then solving for desired circuit parameters using typical analysis techniques. For example, when forward biased, a silicon diode can be thought of as a fixed 0.7 volt drop, and then KVL and KCL can be applied as needed. The polarity of the device is typically denoted by a band placed closest to the cathode.

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7.1.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(2) Signal diodes (1N4148, 1N914)

(1) 1 k Ω resistor 1/4 watt

actual: _____

(1) 10 k Ω resistor 1/4 watt

actual: _____

(1) 4.7 k Ω resistor 1/4 watt

actual: _____

1N4148/1N914 Datasheet: https://www.onsemi.com/pub/Collateral/1N914-D.PDF

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7.1.3: Schematics

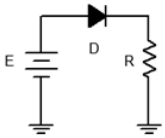


Figure 7.1.3.1

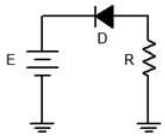


Figure 7.1.3.2

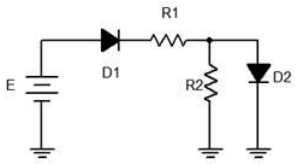


Figure 7.1.3.3

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7.1.4: Procedure

7.1.4.1 3.4.1: Forward Curve

1. Consider the circuit of Figure 3.3.1 using R = 1 kΩ. For any positive value of E, the diode should be forward biased. Once E exceeds the knee voltage, all of E (minus approximately 0.7 volts) drops across R. Thus, as E increases, so does the diode current.

2. Build the circuit of Figure 3.3.1 using R = 1 kΩ. Set E to 0 volts and measure both the diode's voltage and current and record the results in Table 3.5.1. Remember, voltage is measured across a device (parallel) while current is measured through it (series). Repeat this process for the remaining source voltages listed.

3. From the data collected in Table 3.5.1, plot the current versus voltage characteristic of the forward biased diode. Make sure V_D is the horizontal axis with I_D on the vertical.

7.1.4.2 3.4.2: Reverse Curve

4. Consider the circuit of Figure 3.3.2 using R = 1 kΩ. For any positive value of E, the diode should be reversed biased. In this case, the diode should always behave like an open switch and thus no current should flow. If no current flows, the voltage across R should be zero, and thus the diode voltage should be equal to the applied source voltage. Note that the diode's voltage polarity is negative with respect to that of Figure 3.3.1.

5. Build the circuit of Figure 3.3.2 using R = 1 kΩ. Set E to 0 volts and measure both the diode's voltage and current and record the results in Table 3.5.2. Repeat this process for the remaining source voltages listed.

6. From the data collected in Table 3.5.2, plot the current versus voltage characteristic of the reverse biased diode. Make sure V_D is the horizontal axis with I_D on the vertical.

7.1.4.3 3.4.3: Practical Analysis

7. Consider the circuit of Figure 3.3.3 using E = 12 volts, R1 = 10 kΩ and R2 = 4.7 kΩ. Analyze the circuit using the ideal 0.7 volt forward drop approximation and determine the voltages across the two resistors. Record the results in the first two columns of the first row (Variation 1) of Table 3.5.3.

8. Build the circuit of Figure 3.3.3 using E = 12 volts, R1 = 10 kΩ and R2 = 4.7 kΩ. Measure the voltages across the two resistors. Record the results in columns three and four of the first row (Variation 1) of Table 3.5.3. Also compute and record the percent deviations in columns four and five.

9. Reverse the direction of D1 and repeat steps 7 and 8 as Variation 2 in Table 3.5.3.

10. Return D1 to the original orientation and reverse the direction of D2. Repeat steps 7 and 8 as Variation 3 in Table 3.5.3.

11. Reverse the direction of both D1 and D2, and repeat steps 7 and 8 as Variation 4 in Table 3.5.3.

7.1.4.4 3.4.4: Computer Simulation

12. Repeat steps 7 through 11 using a simulator, recording the results in Table 3.5.4.

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7.1.5: Data Tables

E (volts)	V_D	I_D
0		0
0.5		
1		
2		
4		
6		
8		
10		

Table 7.1.5.1

E (volts)	V_D	I_D
0		
1		
2		
5		
10		
15		

Table 7.1.5.2

Variation	$V_{R1\ Theory}$	Extra close brace or missing open brace	$V_{R1\ Exp}$	$V_{R2\ Exp}$	% Dev V_{R1}	% Dev V_{R2}
1						
2						
3						
4						

Table 7.1.5.3

Variation	$V_{R1\ Sim}$	$V_{R2\ Sim}$
1		
2		
3		
4		

Table 7.1.5.4

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7.1.6: Questions

1. Is 0.7 volts a reasonable approximation for a forward bias potential? Is an open circuit a reasonable approximation for a reverse biased diode? Support your arguments with experimental data.

2. The “average” resistance of a forward biased diode can be computed by simply dividing the diode's voltage by its current. Using Table 3.5.1, determine the smallest average diode resistance (show work).

3. The instantaneous resistance (also known as AC resistance) of a diode may be approximated by taking the differences between adjacent current-voltage readings. That is, $r_{diode} = \Delta V_{diode} / \Delta I_{diode}$. What are the smallest and largest resistances using Table 3.5.1 (show work)? Based on this, what would a plot of instantaneous diode resistance versus diode current look like?

4. If the circuit of Figure 3.3.3 had been constructed with LEDs in place of switching diodes, would there be any changes to the values measured in Table 3.5.3? Why/why not?

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SECTION OVERVIEW

7.2: Light Emitting Diodes

Objective

This exercise examines the general performance and use of light emitting diodes. This includes forward bias and reverse bias characterization along with brightness variation.

7.2.1: Theory Overview

7.2.2: Equipment

7.2.3: Schematics

7.2.4: Procedure

7.2.5: Data Tables

7.2.6: Questions

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7.2.1: Theory Overview

The LED is similar to the ordinary signal or rectifying diode in that it is polarity sensitive. In reverse bias the device behaves as an open and prevents current flow. In forward bias, the device allows current flow once its forward barrier potential is reached. This potential is significantly higher than that of ordinary diodes and depends on the material used, and hence, the color that is displayed. Generally, luminous intensity is a function of the forward current. That is, the greater the current, the brighter the output. In operation, a series limiting resistor or other control device must be used to limit the forward current and prevent damage that could occur to the LED from excessive current. Different technologies are used in the design and production of LEDs and there are many variations including full spectrum (white) and high brightness versions. The cathode of an LED is typically denoted by a flat spot on the plastic casing and/or by the shorter of the two leads.

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7.2.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(1) Each of standard LEDs of various colors (red, blue, green, yellow)

(1) High brightness white LED

(1) 1 k Ω resistor 1/4 watt

actual: _____

Standard red LED Datasheet:

https://www.sparkfun.com/datasheets/...R531R3D-D2.pdf

High brightness white LED Datasheet:

http://cdn.sparkfun.com/datasheets/C...1042WC-D15.pdf

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7.2.3: Schematics

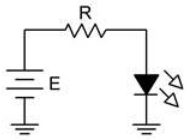


Figure 7.2.3.1

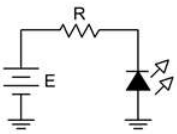


Figure 7.2.3.2

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7.2.4: Procedure

7.2.4.1 4.4.1: Forward Curve

1. Consider the circuit of Figure 4.3.1 using R = 1 kΩ. For any positive value of E, the diode should be forward biased. Once E exceeds the knee voltage, the difference between the source and the knee drops across R. Thus, as E increases, so does the LED current and hence its brightness.

2. Build the circuit of Figure 4.3.1 using R = 1 kΩ and the red LED. Set E to 0 volts and measure both the LED voltage and current and record the results in Table 4.5.1. Note the relative brightness level. Repeat this process for the remaining source voltages listed.

3. From the data collected in Table 4.5.1, plot the current versus voltage characteristic of the forward biased LED. Make sure V_D is the horizontal axis with I_D on the vertical.

4. Repeat steps 2 and 3 for the blue LED using Table 4.5.2.

5. If other colors are available repeat steps 2 and 3 for them using Table 4.5.3 (create other tables as needed).

7.2.4.2 4.4.2: High Brightness

6. Replace the LED of Figure 4.3.1 with the high brightness white LED. Set the supply to 12 volts. Record the LED voltage, current and brightness in Table 4.5.4.

7.2.4.3 4.4.3: Reverse Curve

7. Consider the circuit of Figure 4.3.2 using R = 1 kΩ. For any positive value of E, the LED should be reversed biased. In this case, the LED should always be open causing no current to flow. If no current flows, the LED produces no light. Also, the voltage across R should be zero, and thus the LED voltage should be equal to the applied source voltage. Note that the LED voltage polarity is negative with respect to that of Figure 4.3.1.

8. Build the circuit of Figure 4.3.2 using R = 1 kΩ using the red LED. Set E to 0 volts and measure both the LED voltage and current and record the results in Table 4.5.5. Repeat this process for the remaining source voltages listed.

9. From the data collected in Table 4.5.5, plot the current versus voltage characteristic of the reverse biased diode. Make sure V_D is the horizontal axis with I_D on the vertical.

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7.2.5: Data Tables

E (volts)	V_D	I_D	Brightness
0			
1			
2			
3			
4			
6			
12			

Table 7.2.5.1: Color - Red

E (volts)	V_D	I_D	Brightness
0			
1			
2			
3			
4			
6			
12			

Table 7.2.5.2: Color - Blue

E (volts)	V_D	I_D	Brightness
0			
1			
2			
3			
4			
6			
12			

Table 7.2.5.3: Color -

E (volts)	V_D	I_D	Brightness
12			

Table 7.2.5.4: High Brightness

E (volts)	V_D	I_D
0		
1		
3		
8		

Table 7.2.5.5

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7.2.6: Questions

1. Is the forward knee voltage of an LED comparable to that of ordinary switching and rectifying diodes?

2. Are the knee voltages of LEDs consistent across colors?

3. Compare the reverse characteristics of LEDs and switching diodes.

4. What can be said regarding LED brightness and current?

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SECTION OVERVIEW

7.3: Photodiodes

Objective

The objective of this exercise is to examine the operation of the photodiode in both the photovoltaic and photoconductive modes.

7.3.1: Theory Overview

7.3.2: Equipment

7.3.3: Schematics

7.3.4: Procedure

7.3.5: Data Tables

7.3.6: Questions

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7.3.1: Theory Overview

The photodiode is, in essence, the reverse of the LED. In fact, depending on their design, LEDs can be used as a type of photodiode. Photodiodes are responsive to light in one of two ways. The first method is the photovoltaic mode. In this mode, a voltage appears across the PN junction that is proportional to the amount of light striking it. It can be thought of as a small voltage source or battery. The second mode is photoconductive. In this mode, the photodiode is reverse biased by an external DC supply. The amount of current flowing through the diode will be proportional to the amount of light striking the junction. Typically, this current will pass through a series resistor to create a voltage or it can be sent into a current amplifier circuit.

A photo emitter/detector pair is a pairing of an LED and a photodiode that are designed to produce and detect the same wavelength of light. The wavelength of light may be outside the range of the human visible spectrum. Infrared (IR) is often used for consumer remote control devices. Emitter/detector pairs might use a phototransistor in place of a photodiode. The performance is similar except that photodiodes tend to have a quicker response while phototransistors tend to produce higher currents.

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7.3.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(1) Non-diffuse light source (pen light)

(1) Yellow LED (1) Blue LED

(1) IR emitter/detector pair (Lite-On LTE-302 emitter, LTR-301 detector)

(1) 470 Ω resistor 1/4 watt

actual: _____

(1) 33 k Ω resistor 1/4 watt

actual: _____

IR Emitter Datasheet: http://optoelectronics.liteon.com/up...-0009/E302.pdf

IR Detector Datasheet: http://optoelectronics.liteon.com/up...13/LTR-301.pdf

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7.3.3: Schematics

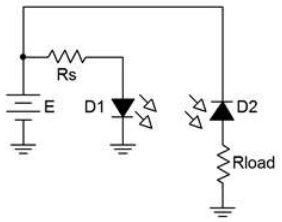


Figure 7.3.3.1

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7.3.4: Procedure

7.3.4.1 5.4.1: LED as Detector

1. Most LEDs can be used as light detectors. In photovoltaic mode, the output potential is a function of the light level and the make-up of the device (i.e., typically its color). Insert a yellow LED into a protoboard with nothing obstructing it. Place a DMM across it and measure the resulting DC voltage, recording it in Table 5.3.1 under “Normal”.

2. Shade the LED so that minimal light strikes it and measure the resulting voltage. Record the value in Table 5.3.1 under “Dark”.

3. Using the pen light, illuminate the LED from a distance of approximately 10 centimeters, measure and record the voltage in Table 5.3.1 under “Bright”. Also, slowly vary the distance of the pen light from a few centimeters to 20 or so and note what happens to the voltage.

4. Replace the yellow LED with the blue LED and repeat steps 1 through 3.

7.3.4.2 5.4.2: IR Emitter/Detector Pair

5. Figure 5.3.1 shows an emitter/detector pair. These devices will emit and detect light at the same wavelength and tend to not produce or detect light at other wavelengths. This aids in avoiding interference. The detector is configured in photoconductive mode. Its current will increase with increasing light level. This current also flows through Rload meaning that Vload will be proportional to light level.

6. Build the circuit of Figure 5.3.1 using E = 7 volts, Rs = 470 Ω and Rload = 33 kΩ. The emitter diode is denoted with a yellow dot on its case while the detector diode shows a red dot. It is very important that the pair properly be aligned. The bubbles should face each other and cases should be at same height, effectively aiming one bubble at the other. Further, they should only be a few millimeters apart. Finally, the short leads indicate the cathodes.

7. Energize the circuit. Because this pair operates in the infrared, nothing will be apparent to the human eye. Verify that the emitter is operating by measuring the voltage across it. It should be in the vicinity of 1.1 volts.

8. Measure Vload and record the value in Table 5.3.2.

9. Slip an opaque card such as a thin piece of black plastic or cardboard between the emitter/detector pair. Measure and record Vload in Table 5.3.2.

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7.3.5: Data Tables

Variation	$V_{LED-YELLOW}$	$V_{LED-BLUE}$
Normal		
Dark		
Bright		

Table 7.3.5.1

Variation	V_{LOAD}
Open	
Blocked	

Table 7.3.5.2

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7.3.6: Questions

1. What is the effect of light intensity on the LED when used in photovoltaic mode?

2. What influence does the color of the LED have on the voltage produced when used in photovoltaic mode?

3. What is the correlation between Vload and light level in Figure 5.3.1? Give at least two examples of where this effect might be put to good use.

4. Why might an infrared emitter/detector system be used in consumer electronics in place of ordinary visible light emitter/detectors?

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SECTION OVERVIEW

7.4: The Zener Diode

Objective

The objective of this exercise is to examine the operation of the Zener diode and to plot its characteristic curve.

7.4.1: Theory Overview

7.4.2: Equipment

7.4.3: Schematics

7.4.4: Procedure

7.4.5: Data Tables

7.4.6: Questions

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7.4.1: Theory Overview

When forward biased, the Zener diode behaves similarly to an ordinary switching diode, that is, it incurs a 0.7 volt drop for silicon devices. Unlike a switching diode, the Zener is normally placed in reverse bias. If the circuit potential is high enough, the Zener will exhibit a fixed voltage drop. This is called the Zener potential or V_Z. Manufacturer's specify this voltage with respect to the Zener test current, or I_{ZT}; a point past the knee of the voltage-current curve. That is, if the Zener's current is at least equal to I_{ZT}, then its voltage is approximately equal to the rated V_Z. Above this current, even very large increases in current will produce only very modest changes in voltage. Therefore, for basic circuit analysis, the Zener can be replaced mathematically by a fixed voltage source equal to V_Z. In practice, some series resistance is usually required to limit the current to a value below the Zener's maximum in order to prevent damage.

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7.4.2: Equipment

(1) Adjustable DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(1) Zener diode around 5.1 volts (NZX5V1B, 1N751)

(1) 2.2 k Ω resistor 1/4 watt

actual: _____

(1) 4.7 k Ω resistor 1/4 watt

actual: _____

NZX5V1B Datasheet: https://assets.nexperia.com/document...et/NZX_SER.pdf

1N751 Datasheet: www.digitroncorp.com/Document...N759A,-1N4370- 1N4372A.aspx?ext=.pdf

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7.4.3: Schematics

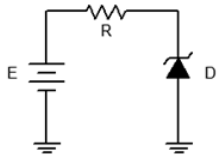


Figure 7.4.3.1

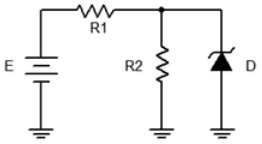


Figure 7.4.3.2

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7.4.4: Procedure

7.4.4.1 6.4.1: Reverse Curve

1. Consider the circuit of Figure 6.3.1 using R = 2.2 kΩ. For any positive value of E the Zener is reverse biased. Until the Zener potential is reached, the diode resistance is effectively infinite and thus no current flows. In this case the voltage across R is zero due to Ohm's law. Consequently, all of E should appear across the Zener. Once the source exceeds the Zener voltage, the remainder of E (i.e. E minus the Zener potential) drops across R. Thus, as E increases, the circulating current increases but the voltage across the zener remains steady.

2. Build the circuit of Figure 6.3.1 using R = 2.2 kΩ. Set E to 0 volts and measure both the diode's voltage and current and record the results in Table 6.5.1. Repeat this process for the remaining source voltages listed.

3. From the data collected in Table 6.5.1, plot the current versus voltage characteristic of the reverse biased diode. Make sure V_D is the horizontal axis with I_D on the vertical.

7.4.4.2 6.4.2: Practical Analysis

4. Consider the circuit of Figure 6.3.2 using R1 = 2.2 kΩ and R2 = 4.7 kΩ. In general, to analyze circuits like this, first assume that the Zener is out of the circuit and then compute the voltage across R2 using the voltage divider rule. If the resulting voltage is less than the Zener potential then the Zener is inactive (high resistance) and does not affect the circuit. If, on the other hand, the resulting voltage is greater than the Zener potential then the Zener is active and will limit the voltage across R2 to V_Z. Via KVL, the remainder of the voltage drops across R1 and from this the supply current may be determined. This current will then split between R2 and the Zener. The R2 current is found using Ohm's law. The Zener current is then found via KCL. Note that for higher and higher values of E, the voltage across (and therefore the current through) R2 does not change. Instead, all of the "excess" current from the source passes through the Zener.

5. Build the circuit of Figure 6.3.2 using R1 = 2.2 kΩ and R2 = 4.7 kΩ. Set E to 2 volts. Compute the theoretical diode voltage and current, and record them in the first row of Table 6.5.2. Then measure the diode current and voltage and record in Table 6.5.2. Finally, compute and record the deviations.

6. Repeat step 5 for the remaining source voltages in Table 6.5.2.

7.4.4.3 6.4.3: Computer Simulation

7. Repeat steps 5 and 6 using a simulator, recording the results in Table 6.5.3.

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7.4.5: Data Tables

E (volts)	V_D	I_D
0		
1		
2		
5		
10		
15		
20		

Table 7.4.5.1

E (volts)	$V_{D\ Theory}$	$I_{D\ Theory}$	$V_{D\ Exp}$	$I_{D\ Exp}$	% Dev V_D	% Dev I_D
2						
5						
10						
15						
20						

Table 7.4.5.2

E (volts)	$V_{D\ Sim}$	$I_{D\ Sim}$
2		
5		
10		
15		
20		

Table 7.4.5.3

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7.4.6: Questions

1. Is it safe to assume that the voltage across a Zener is always equal to the rated V_Z? Why/why not?

2. The instantaneous resistance (also known as AC resistance) of a diode may be approximated by taking the differences between adjacent current-voltage readings. That is, $r_{diode} = \Delta V_{diode}/\Delta I_{diode}$. What is the smallest effective resistance of the Zener using Table 6.5.1 (show work)?

3. If the circuit of Figure 6.3.1 had been constructed with the Zener flipped, how would this effect the results recorded in Table 6.5.1?

4. Assume that a diode with a much higher I_{ZT} rating (say, 100 mA) was used in this exercise. In general, what would the likely outcome be for the circuit of Figure 6.3.2?

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SECTION OVERVIEW

7.5: Half-wave Rectifier

Objective

The goal of this exercise is to investigate the ideal versus real operation of a basic half-wave rectifier. The effects of a filtering capacitor are included.

7.5.1: Theory Overview

7.5.2: Equipment

7.5.3: Schematics

7.5.4: Procedure

7.5.5: Data Tables

7.5.6: Questions

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7.5.1: Theory Overview

The primary function of a rectifier is to turn an incoming AC waveform into a pulsating DC waveform. This can be achieved by simply blocking one of the two polarities from reaching the load. This is called a half-wave rectifier. A rectifier might be used as part of an AC to DC power supply but might also be used as part of a signal processing system. Ideally, a diode will behave as either an open or a closed switch depending on the polarity of the applied signal. This means that one polarity can be allowed through while the other can be blocked, perfect for this situation. In reality, the diode will require a forward turnon potential which results in a portion of the allowed signal being lost (e.g., the first 0.7 volts will be lost when using a silicon device). This fact makes a simple diode rectifier ineffective when used with very small signal amplitudes. Finally, in order to “fill the gap” where the blocked polarity would have been, a capacitor can be used to store some of the energy at the peak to be released during the gap. The higher the capacitance value, the more effective the smoothing will be.

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7.5.2: Equipment

(1) Dual channel oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(1) Signal diode (1N914, 1N4148)

(1) 10 k Ω resistor 1/4 watt

actual: _____

(1) 22 nF capacitor

actual: _____

(1) 470 nF capacitor

actual: _____

1N4148/1N914 Datasheet: https://www.onsemi.com/pub/Collateral/1N914A-D.pdf

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7.5.3: Schematics

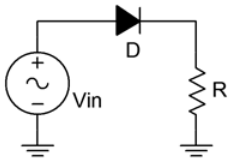


Figure 7.5.3.1

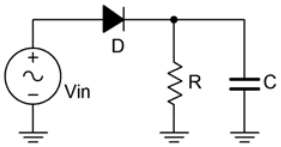


Figure 7.5.3.2

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7.5.4: Procedure

7.5.4.1 11.4.1: Simple Rectifier

1. Consider the circuit of Figure 11.3.1. For an input voltage significantly larger than 0.7 volts, the diode will be forward biased for the positive half of the input sine wave. Therefore, all of the input signal (less 0.7 volts) will appear across the load resistor, R. Conversely, during the negative polarity of the input, the diode will be open, thus blocking any current and producing no voltage across the load.

2. Build the circuit of Figure 11.3.1 using Vin = 10 volts peak at 1 kHz and R = 10 kΩ. Set the oscilloscope inputs to DC coupled. Place one oscilloscope probe across the input generator and a second probe across the load resistor. Record the peak amplitude of the output load waveform in Table 11.5.1. Also, save an image of the scope trace showing both the input and output waveforms.

3. Measure the load voltage with the DMM (DC volts) and record this in Table 11.5.1.

4. Reverse the diode and repeat steps 2 and 3.

5. Reverse the diode so that it is back to the original orientation. Reduce the input to 800 mV peak and repeat step 2.

7.5.4.2 11.4.2: Filter Capacitor

6. The circuit of Figure 11.3.2 adds a filtering capacitor across the load. This should help to “fill the gaps” created by the missing portions of the waveform. Build the circuit of Figure 11.3.2 using Vin = 10 volts peak at 1 kHz, R = 10 kΩ and C = 22 nF. Making sure that the scope inputs are DC coupled, place scope probes across the input and load, and capture the resulting image. Record the peak value in Table 11.5.2.

7. Measure the load voltage with the DMM (DC volts) and record this in Table 11.5.2.

8. Replace C with the 470 nF capacitor and repeat steps 5 and 6.

7.5.4.3 11.4.3: Computer Simulation

9. Perform a Transient Analysis simulation of the circuits shown in Figures 11.3.1 and 11.3.2, and compare the resulting waveforms to those captured from the oscilloscope.

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7.5.5: Data Tables

Variation	V_{load} peak	DMM DCV
Original		
Reversed Diode		
800 mV Input		X

Table 7.5.5.1

Capacitor	V_{load} peak	DMM DCV
22 nF		
470 nF		

Table 7.5.5.2

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7.5.6: Questions

1. How well do the peak values of the load voltage track the peak values of the input voltage?

2. What are the limits of the half-wave circuit at rectifying small amplitude signals? What might be done to improve its effectiveness?

3. What is the effect of reversing the orientation of the diode? How does this affect the DC value measured by the DMM?

4. What is the effect of adding capacitance to the circuit? How does this affect the DC value measured by the DMM?

5. How would the waveforms differ if the oscilloscope inputs had been AC coupled instead of DC coupled?

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CHAPTER OVERVIEW

8: Transistors

8.1: Bipolar Junction Transistor- Base Bias - CE Configuration

8.1.1: Theory Overview

8.1.2: Equipment

8.1.3: Schematics

8.1.4: Procedure

8.1.5: Data Tables

8.1.6: Questions

8.2: Emitter Bias

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8.2.3: Schematics

8.2.4: Procedure

8.2.5: Data Tables

8.2.6: Questions

8.3: Voltage Divider Bias

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8.3.2: Equipment

8.3.3: Schematics

8.3.4: Procedure

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8.3.6: Questions

8.4: Feedback Biasing

8.4.1: Theory Overview

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8.4.3: Schematics

8.4.4: Procedure

8.4.5: Data Tables

8.4.6: Questions

8.5: PNP Transistors

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8.5.2: Equipment

8.5.3: Schematics

8.5.4: Procedure

8.5.5: Data Tables

8.5.6: Questions

8.6: Common Emitter Amplifier

8.6.1: Theory Overview

8.6.2: Equipment

8.6.3: Schematics

8.6.4: Procedure
8.6.5: Data Tables
8.6.6: Questions

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SECTION OVERVIEW

8.1: Bipolar Junction Transistor- Base Bias - CE Configuration

Objective

The objective of this exercise is to explore the operation of a basic common emitter biasing configuration for bipolar junction transistors, namely fixed base bias. Along with the general operation of the transistor and the circuit itself, circuit stability with changes in beta is also examined.

8.1.1: Theory Overview

8.1.2: Equipment

8.1.3: Schematics

8.1.4: Procedure

8.1.5: Data Tables

8.1.6: Questions

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8.1.1: Theory Overview

For a bipolar junction transistor to operate properly, the base-emitter junction must be forward biased while the collector-base junction must be reverse biased. This will place V_{BE} at approximately 0.7 volts and the collector current I_C will be equal to the base current I_B times the current gain $beta$. For small signal devices, the current gain is greater than 100 typically. Thus, $I_C \gg I_B$ and $I_C \approx I_E$.

The common emitter configuration places the emitter terminal at ground. The base terminal is seen as the input and the collector as the output. Using a fixed base supply, the base current is dependent on the value of the base resistor via Ohm's law. Consequently, any variation in current gain across a batch of transistors will show up as an equivalent variation in collector current, and by extension, a variation in collector-emitter voltage V_{CE}.

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8.1.2: Equipment

(1) Dual adjustable DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(3) Small signal NPN transistors (2N3904)

(1) 1.2 k Ω resistor 1/4 watt

actual: _____

(1) 330 k Ω resistor 1/4 watt

actual: _____

2N3904 Datasheet: https://www.onsemi.com/pub/Collateral/2N3903-D.PDF

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8.1.3: Schematics

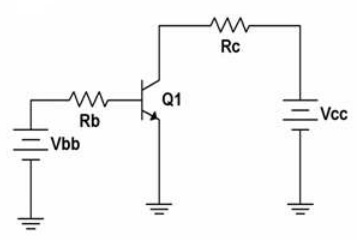


Figure 8.1.3.1

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8.1.4: Procedure

8.1.4.1 15.4.1: A Quick Check

1. A quick and easy way to determine if a transistor is damaged is through the use of the resistance (or diode) function of a multimeter. The multimeter will produce a small current in order to determine the connected resistance value. This current is sufficient to partially forward or reverse bias a PN junction. Thus, for an NPN device, placing the red lead on the base and the black lead on the emitter and collector in turn will produce forward bias on the junctions and the meter will show a low resistance. Reversing the leads will create reverse bias and a high resistance will be indicated. If the leads are connected from collector to emitter, one of the two junctions will be reverse biased regardless of lead polarity, and thus, a high resistance is always indicated. Before proceeding to the next step, check the three transistors using this method to ensure that they are functioning. (Note: some multimeters include a “beta checker” function. This may also be used to determine if the devices are good but the beta value produced should not be considered precise as the measurement current and voltage are most likely different from the circuit in which the transistor will be used.)

8.1.4.2 15.4.2: Base Bias

2. Consider the circuit of Figure 15.3.1 with Vbb = 11V, Vcc = 15V, Rb = 330 kΩ and Rc = 1.2 kΩ. Assume V_{BE} = 0.7 volts. Further, assume that beta is 150 (a typical value for this device in this application). Calculate the expected values of I_B, I_C and I_E, and record them in the “Theory” columns of Table 15.5.1. Note that the theoretical values will be the same for all three transistors.

3. Based on the expected value of I_C, determine the theoretical value of V_{CE} and record it in Table 15.5.2. Also, fill in Table 15.5.2 with the typical (theoretical) beta value of 150.

4. Build the circuit of Figure 15.3.1 with Vbb = 11V, Vcc = 15V, Rb = 330 kΩ and Rc = 1.2 kΩ. Measure and record the base, collector and emitter currents, and record them in the first row of Table 15.5.1. Find the deviations between the theoretical and experimental currents, and record these in Table 15.5.1.

5. Measure the base-emitter and collector-emitter voltages and record in the first row of Table 15.5.2. Based on the measured values of base and collector current from Table 15.5.1, calculate and record the experimental betas in Table 15.5.2. Finally, compute and record the deviations for the voltages and for the current gain in Table 15.5.2.

6. Remove the first transistor and replace it with the second unit. Repeat steps four and five using the second row of Tables 15.5.1 and 15.5.2.

7. Remove the second transistor and replace it with the third unit. Repeat steps four and five using the third row of Tables 15.5.1 and 15.5.2.

8.1.4.3 15.4.3: Design

8. One way of improving the circuit of Figure 15.3.1 is to redesign it so that a single power supply may be used. As noted previously, the base current is largely dependent on the value of V_{BB} and R_B. If the supply is changed, the resistance can be changed by a similar factor in order to keep the base current constant. This is just an application of Ohm’s law. Based on this, determine a new value for R_B that will produce the original I_B if V_{BB} is increased to the V_{CC} value (i.e., a single power supply is used). Record this value in Table 15.5.3.

9. Rewire the circuit so that the original R_B is replaced by the new calculated value (the nearest standard value will suffice). Also, the V_{BB} supply should be removed and the left side of R_B connected to the V_{CC} supply. Measure the new base current and record it in Table 15.5.3. Also determine and record the deviation between the measured and target base current values.

8.1.4.4 15.4.4: Computer Simulation

10. Build the original circuit in a simulator. Run a single simulation and record the I_B, I_C, I_E and V_{CE} values in Table 15.5.4.

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8.1.5: Data Tables

Transistor	I_B Theory	I_B Exp	%D I_B	I_C Theory	I_C Exp	%D I_C	I_E Theory	I_E Exp	%D I_E
1									
2									
3									

Table 8.1.5.1

Transistor	$V_{BE\ Thry}$	$V_{BE\ Exp}$	%D V_{BE}	$V_{CE\ Thry}$	$V_{CE\ Exp}$	%D V_{CE}	β_{Theory}	β_{Exp}	%D β
1									
2									
3									

Table 8.1.5.1

Calculated R_B	Actual R_B Used	I_B Measured	% Deviation I_B

Table 8.1.5.1

$I_{B\ sim}$	$I_{C\ sim}$	$I_{E\ sim}$	$V_{CE\ sim}$

Table 8.1.5.1

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8.1.6: Questions

1. Are the basic transistor parameters borne out in this exercise? That is, are the approximations of V_{BE} = 0.7 and $I_C = I_E$ valid?

2. Is the typical beta value of 150 highly accurate and repeatable?

3. Which circuit parameters are affected by beta changes? Which parameters appear to be immune to changes in beta?

4. Comparing Tables 15.5.1 and 15.5.2, is there a notable pattern between the deviations for beta and collector current? Why/why not?

5. In the circuit of Figure 15.3.1, what must R_B be set to if V_{BB} = 5V and the desired base current is 10 μA?

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SECTION OVERVIEW

8.2: Emitter Bias

Objective

The objective of this exercise is to examine the two supply emitter bias topology and determine whether or not it produces a stable Q point. Various potential troubleshooting issues are also explored.

8.2.1: Theory Overview

8.2.2: Equipment

8.2.3: Schematics

8.2.4: Procedure

8.2.5: Data Tables

8.2.6: Questions

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8.2.1: Theory Overview

One of the problems with simpler biasing schemes such as the base bias is that the Q point (I_C and V_{CE}) will fluctuate with changes in beta. This will result in inconsistent circuit performance. If a fixed voltage can be developed across an emitter resistor, a stable Q point will result. To obtain this fixed emitter resistor voltage, a negative voltage supply may be connected to the low side of the emitter resistor instead of connecting that resistor to ground. The transistor's base is then simply connected back to ground via a single resistor. If this base resistance is relatively small, the base voltage will be close to zero as only the base current flows through it. Consequently, almost all of the negative emitter supply will drop across the emitter resistor, with the exception of the single base-emitter potential. This will result in a stable emitter current, and by extension, stable collector current and collector-emitter voltage. As beta varies, this change will be reflected in a change in base current. This can result in large percentage changes in base voltage; however, the magnitude of the base potential will remain small, and thus, inconsequential.

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8.2.2: Equipment

(1) Dual adjustable DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(3) Small signal transistors (2N3904)

(1) 15 k Ω resistor 1/4 watt

actual: _____

(1) 22 k Ω resistor 1/4 watt

actual: _____

(1) 33 k Ω resistor 1/4 watt

actual: _____

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8.2.3: Schematics

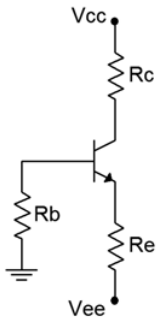


Figure 8.2.3.1

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8.2.4: Procedure

8.2.4.1 17.4.1: DC Load Line

11. Consider the circuit of Figure 17.3.1 using Vcc = 15 volts, Vee = −12 volts, Rb = 33 kΩ, Re = 22 kΩ and Rc = 15 kΩ. Using the approximation of a negligible base voltage, determine the ideal end points of the DC load line and the Q point, and record these in Table 17.5.1.

8.2.4.2 17.4.2: Circuit Voltages and Beta

12. Continuing with the component values indicated in step one, compute the theoretical emitter and collector voltages, and record them in Table 17.5.2 (Theory). For the theoretical base voltage entry, assume a beta of approximately 150 and determine the base current and voltage from the theoretical collector current recorded in the Table 17.5.1.

13. Build the circuit of Figure 17.3.1 using Vcc = 15 volts, Vee = −12 volts, Rb = 33 kΩ, Re = 22 kΩ and Rc = 15 kΩ. Measure the base, emitter and collector voltages and record them in the first row of Table 17.5.2 (Experimental). Compute the deviations between theoretical and experimental and record these in the first row of Table 17.5.2 (% Deviation).

14. Measure the base and collector currents and record these in the first row of Table 17.5.3. Based on these, compute and record the experimental beta as well.

15. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

16. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

8.2.4.3 17.4.3: Design

17. The collector voltage of the circuit can be altered by a variety of means including changing the collector resistance. If the emitter supply and resistance are held constant, the collector voltage is determined by the collector resistance and the collector supply. Redesign the circuit to achieve a collector voltage of approximately 10 volts. Obtain a resistor close to this value, swap out the original collector resistor and measure the resulting voltage. Record the appropriate values in Table 17.5.4.

8.2.4.4 17.4.4: Troubleshooting

18. Return the original collector resistor to the circuit. Consider each of the individual faults listed in Table 17.5.5 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 17.5.5.

8.2.4.5 17.4.5: Computer Simulation

19. Build the circuit of Figure 17.3.1 in a simulator. Run a DC simulation and record the resulting transistor voltages in Table 17.5.6.

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8.2.5: Data Tables

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 8.2.5.1

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$	%D V_B	%D V_E	%D V_C
1									
2									
3									

Table 8.2.5.2

Transistor	I_B	I_C	β
1			
2			
3			

Table 8.2.5.3

$R_{C\ Theory}$	$R_{C\ Actual}$	$V_{C\ Measured}$

Table 8.2.5.4

Issue	V_B	V_E	V_C
R_B Short			
R_B Open			
R_C Short			
R_C Open			
R_E Open			
V_{CE} Open			

Table 8.2.5.5

$V_{B\ Sim}$	
$V_{E\ Sim}$	
$V_{C\ Sim}$	

Table 8.2.5.6

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8.2.6: Questions

1. Based on the results of Table 17.5.1, is the transistor operating in saturation, cutoff or in the linear region?

2. Based on the results of Tables 17.5.2 and 17.5.3, does the circuit achieve a stable operating point when compared to beta?

3. How does the Emitter Bias circuit compare to Base Bias in terms of Q point stability and complexity?

4. Using the original circuit, determine a new value for the emitter resistance that will yield half of the quiescent collector current recorded in Table 17.5.1.

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SECTION OVERVIEW

8.3: Voltage Divider Bias

Objective

The objective of this exercise is to examine the voltage divider bias topology and determine whether or not it produces a stable Q point. Various potential troubleshooting issues are also explored.

8.3.1: Theory Overview

8.3.2: Equipment

8.3.3: Schematics

8.3.4: Procedure

8.3.5: Data Tables

8.3.6: Questions

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8.3.1: Theory Overview

Like Emitter Bias, Voltage Divider Bias seeks to establish a stable Q point by placing a fixed voltage across an emitter resistor. This will result in a stable emitter current, and by extension, stable collector current and collector-emitter voltage. As beta varies, this change will be reflected in a change in base current. With proper design, this change in base current will have little overall impact on circuit performance. One method of obtaining a stable voltage across the emitter resistor is to apply a stiff voltage divider to the base. “Stiff”, in this case, means that the current through the divider resistors should be much higher than the current tapped off of the divider (the current being tapped off is the base current). By doing so, variations in base current will not excessively load the divider and this will lead to a very stable base voltage. The emitter voltage is one base-emitter drop less, and is the potential across the emitter resistor. Hence, the emitter resistor’s voltage will be kept stable.

When troubleshooting, circuit faults often result in either shorted or open components. Typically this will alter the circuit radically and push the Q point into either cutoff or saturation. The fault may also alter the DC load line itself. Once the transistor goes into either cutoff or saturation, normal linear operation will be lost.

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8.3.2: Equipment

(1) Adjustable DC Power Supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(3) Small signal transistors (2N3904)

(1) 3.3 k Ω resistor 1/4 watt

actual: _____

(1) 4.7 k Ω resistor 1/4 watt

actual: _____

(1) 5.6 k Ω resistor 1/4 watt

actual: _____

(1) 10 k Ω resistor 1/4 watt

actual: _____

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8.3.3: Schematics

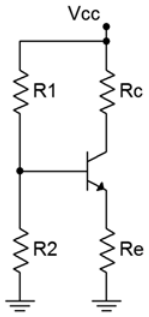


Figure 8.3.3.1

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8.3.4: Procedure

8.3.4.1 18.4.1: DC Load Line

1. Consider the circuit of Figure 18.3.1 using Vcc = 10 volts, R1 = 10 kΩ, R2 = 3.3 kΩ, Re = 4.7 kΩ and Rc = 5.6 kΩ. Using the approximation of a lightly loaded “stiff” voltage divider, determine the ideal end points of the DC load line and the Q point, and record these in Table 18.5.1.

8.3.4.2 18.4.2: Circuit Voltages and Beta

2. Continuing with the component values indicated in step one, compute the theoretical base, emitter and collector voltages, and record them in Table 18.5.2 (Theory).

3. Build the circuit of Figure 18.3.1 using Vcc = 10 volts, R1 = 10 kΩ, R2 = 3.3 kΩ, Re = 4.7 kΩ and Rc = 5.6 kΩ. Measure the base, emitter and collector voltages and record them in the first row of Table 18.5.2 (Experimental). Compute the deviations between theoretical and experimental and record these in the first row of Table 18.5.2 (% Deviation).

4. Measure the base and collector currents and record these in the first row of Table 18.5.3. Based on these, compute and record the experimental beta as well.

5. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

6. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

8.3.4.3 18.4.3: Design

7. The collector current of the circuit can be altered by a variety of means including changing the emitter resistance. If the base voltage is held constant, the collector current is determined by the emitter resistance via Ohm’s law. Redesign the circuit to achieve half of the quiescent collector current recorded in Table 18.5.1. Obtain a resistor close to this value, swap out the original emitter resistor and measure the resulting current. Record the appropriate values in Table 18.5.4.

8.3.4.4 18.4.4: Troubleshooting

8. Return the original emitter resistor to the circuit. Consider each of the individual faults listed in Table 18.5.5 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 18.5.5.

8.3.4.5 18.4.5: Computer Simulation

9. Build the circuit of Figure 18.3.1 in a simulator. Run a DC simulation and record the resulting transistor voltages in Table 18.5.6.

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8.3.5: Data Tables

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 8.3.5.1

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$	%D V_B	%D V_E	%D V_C
1									
2									
3									

Table 8.3.5.2

Transistor	I_B	I_C	β
1			
2			
3			

Table 8.3.5.3

$R_{E\ Theory}$	$R_{E\ Actual}$	$I_{C\ Measured}$

Table 8.3.5.4

Issue	V_B	V_E	V_C
R_2 Short			
R_E Open			
R_C Short			
R_C Open			
V_{CE} Short			
V_{CE} Open			

Table 8.3.5.5

$V_{B\ Sim}$	
$V_{E\ Sim}$	
$V_{C\ Sim}$	

Table 8.3.5.6

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8.3.6: Questions

1. Based on the results of Table 18.5.1, is the transistor operating in saturation, cutoff or in the linear region?

2. Based on the results of Tables 18.5.2 and 18.5.3, does the circuit achieve a stable operating point when compared to beta?

3. Based on the measurements of Table 18.5.5, is it possible for different circuit problems to produce similar or even identical voltages in the circuit, or is every fault unique in its outcome?

4. What is the required design condition for the voltage divider bias to achieve high Q point stability in spite of changes in beta?

5. Using the original circuit, determine a new value for the collector resistance that will yield a collector voltage of approximately half of the power supply value.

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SECTION OVERVIEW

8.4: Feedback Biasing

Objective

The objective of this exercise is to examine two kinds of feedback biasing: collector feedback and emitter feedback. Both forms potentially are more stable than simple base bias in terms of the impact of beta on collector current.

8.4.1: Theory Overview

8.4.2: Equipment

8.4.3: Schematics

8.4.4: Procedure

8.4.5: Data Tables

8.4.6: Questions

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8.4.1: Theory Overview

By inserting a resistor in either the emitter or collector portions of the transistor circuit, it is possible to partially control the base current in such a way that an increase in beta will cause a decrease in base current which in turn helps to mitigate the tendency of collector current to increase. This will result in circuits that have greater Q point stability than simple base bias circuits although for certain practical reasons they might not be as stable as voltage divider or dual supply emitter bias schemes.

In the collector feedback arrangement, the base resistor is connected from the collector to the base. Therefore, its voltage is one base-emitter drop less than the collector voltage. The collector voltage, in turn, is simply the supply potential minus the collector resistor's drop. Therefore, as the collector current rises, the collector resistor's drop increases, forcing the collector voltage down and thus reducing the base resistor's voltage. By Ohm's law, this means that the base current must decrease. This decrease helps to limit the overall increase in collector current.

The emitter feedback situation is similar. In this instance, as collector current increases the drop across the emitter resistor rises. This will result in an increase in base voltage as it is locked to one base-emitter drop above the emitter. Consequently, as the collector current increases, the voltage across the base resistor decreases which helps to compensate for the original increase in collector current.

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8.4.2: Equipment

(1) Adjustable DC Power Supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(3) Small signal transistors (2N3904)

(1) 330 Ω resistor 1/4 watt

actual: _____

(1) 470 Ω resistor 1/4 watt

actual: _____

(1) 1 k Ω resistor 1/4 watt

actual: _____

(1) 220 k Ω resistor 1/4 watt

actual: _____

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8.4.3: Schematics

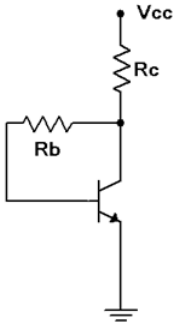


Figure 8.4.3.1



Figure 8.4.3.2

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8.4.4: Procedure

8.4.4.1 19.4.1: Collector Feedback - DC Load Line

1. Consider the circuit of Figure 19.3.1 using Vcc = 12 volts, Rb = 220 kΩ and Rc = 1 kΩ. Determine the ideal end points of the DC load line and the Q point, and record these in Table 19.5.1.

8.4.4.2 19.4.2: Circuit Voltages and Beta

2. Continuing with the component values indicated in step one, compute the theoretical base, emitter and collector voltages, and record them in Table 19.5.2 (Theory).

3. Build the circuit of Figure 19.3.1 using Vcc = 12 volts, Rb = 220 kΩ and Rc = 1 kΩ. Measure the base, emitter and collector voltages and record them in the first row of Table 19.5.2 (Experimental).

4. Measure the base and collector currents and record these in the first row of Table 19.5.3. Based on these, compute and record the experimental beta as well.

5. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

6. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

8.4.4.3 19.4.3: Stability

7. Based on the measurements of Table 19.5.3, determine the maximum percent change of collector current and record in Table 19.5.4. Also determine the maximum percent change of beta and record in Table 19.5.4.

8.4.4.4 19.4.4: Emitter Feedback - DC Load Line

8. Consider the circuit of Figure 19.3.2 using Vcc = 12 volts, Rb = 220 kΩ, Re = 470 Ω and Rc = 330 Ω. Determine the ideal end points of the DC load line and the Q point, and record these in Table 19.5.5.

8.4.4.5 19.4.5: Circuit Voltages and Beta

9. Continuing with the component values indicated in step one, compute the theoretical base, emitter and collector voltages, and record them in Table 19.5.6 (Theory).

10. Build the circuit of Figure 19.3.2 using Vcc = 12 volts, Rb = 220 kΩ, Re = 470 Ω and Rc = 330 Ω. Measure the base, emitter and collector voltages and record them in the first row of Table 19.5.6 (Experimental).

11. Measure the base and collector currents and record these in the first row of Table 19.5.7. Based on these, compute and record the experimental beta as well.

12. Swap the transistor with the second transistor and repeat steps 3 and 4 using the second rows of the tables.

13. Swap the transistor with the third transistor and repeat steps 3 and 4 using the third rows of the tables.

8.4.4.6 19.4.6: Stability

14. Based on the measurements of Table 19.5.7, determine the maximum percent change of collector current and record in Table 19.5.8. Also determine the maximum percent change of beta and record in Table 19.5.8.

8.4.4.7 19.4.7: Troubleshooting

15. For the emitter feedback bias circuit, consider each of the individual faults listed in Table 19.5.9 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 19.5.9.

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8.4.5: Data Tables

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 8.4.5.1

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$
1						
2						
3						

Table 8.4.5.2

Transistor	I_B	I_C	β
1			
2			
3			

Table 8.4.5.3

% $\Delta\ \beta$	
% $\Delta\ I_C$	

Table 8.4.5.4

$V_{CE\ (Cutoff)}$	
$I_{C\ (Sat)}$	
V_{CEQ}	
I_{CQ}	

Table 8.4.5.5

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$
1						
2						
3						

Table 8.4.5.6

Transistor	I_B	I_C	β
1			
2			
3			

Table 8.4.5.7

% Δ β	
% Δ I_C	

Table 8.4.5.8

Issue	V_B	V_E	V_C
R_B Open			
R_E Open			
R_E Short			
R_C Open			
R_C Short			
V_{CE} Open			

Table 8.4.5.9

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8.4.6: Questions

1. Based on the results of Tables 19.5.4 and 19.5.8, do these circuits achieve a stable operating point when compared to beta?

2. Which circuit is more stable in this exercise; the emitter feedback bias or the collector feedback bias? Is it safe to say that this will always be the case for any emitter feedback bias circuit versus any collector feedback bias circuit?

3. Are the transistor voltages always as stable as the collector current or can they be more or less stable?

4. Based on the collector current equation derivations for the two circuits, derive the collector current equation for a combination circuit which consists of a collector feedback bias circuit with an emitter resistor added.

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SECTION OVERVIEW

8.5: PNP Transistors

Objective

The objective of this exercise is to investigate the practical differences between circuits implemented with PNP transistors versus NPN transistors. PNP versiosn of basic biasing and LED driver circuits will be used.

8.5.1: Theory Overview

8.5.2: Equipment

8.5.3: Schematics

8.5.4: Procedure

8.5.5: Data Tables

8.5.6: Questions

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8.5.1: Theory Overview

On a practical level, PNP transistors may be thought of as a mirror image of their NPN counterparts. That is, all of the device's voltage polarities and current directions will be opposite of those found with NPNs. In fact, a simple way to turn an NPN circuit into an equivalent PNP circuit is to swap out the transistor and then flip the polarity of the power supply (or supplies, as the case may be). The resulting circuit will produce essentially the same voltages and currents as the original but with reversed polarities. By no means are negative power supplies a requirement to use PNPs, though. Commonly, the circuit is “flipped top to bottom” and implemented with a positive supply. In this case the emitter will be found toward the top and the collector toward the bottom. In some instances this orientation may also reverse the operational logic of the circuit. For example, the “flipped” PNP LED driver becomes an inverting driver. That is, a logic low will light the LED instead of a logic high.

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8.5.2: Equipment

(1) Adjustable DC Power Supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(3) Small signal PNP transistors (2N3906)

(1) LED

(1) 220 Ω resistor 1/4 watt

actual: _____

(1) 3.3 k Ω resistor 1/4 watt

actual: _____

(1) 4.7 k Ω resistor 1/4 watt

actual: _____

(1) 5.6 k Ω resistor 1/4 watt

actual: _____

(1) 10 k Ω resistor 1/4 watt

actual: _____

2N3906 Datasheet: https://www.onsemi.com/pub/Collateral/2N3906-D.PDF

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8.5.3: Schematics

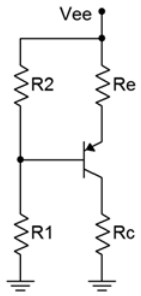


Figure 8.5.3.1

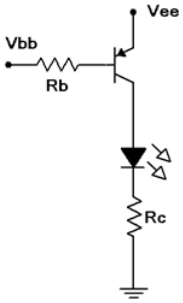


Figure 8.5.3.2

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8.5.4: Procedure

8.5.4.1 20.4.1: PNP Voltage Divider

1. Consider the circuit of Figure 20.3.1 using Vee = 10 volts, R1 = 10 kΩ, R2 = 3.3 kΩ, Re = 4.7 kΩ and Rc = 5.6 kΩ. Using the approximation of a lightly loaded “stiff” voltage divider, determine the theoretical base, emitter and collector voltages, and record them in Table 20.5.1 (Theory).

2. Build the circuit of Figure 20.3.1 using Vee = 10 volts, R1 = 10 kΩ, R2 = 3.3 kΩ, Re = 4.7 kΩ and Rc = 5.6 kΩ. Measure the base, emitter and collector voltages and record them in the first row of Table 20.5.1 (Experimental).

3. Swap the transistor with the second transistor and repeat steps 1 and 2 using the second row of the table.

4. Swap the transistor with the third transistor and repeat steps 1 and 2 using the third row of the table.

8.5.4.2 20.4.2: Troubleshooting

5. Consider each of the individual faults listed in Table 20.5.2 and estimate the resulting base, emitter and collector voltages. Introduce each of the individual faults in turn and measure and record the transistor voltages in Table 20.5.2.

8.5.4.3 20.4.3: PNP LED Driver

6. Consider the PNP saturating switch of Figure 20.3.2 using Vee = Vbb = 5 volts, Rb = 4.7 kΩ and Rc = 220 Ω. Calculate the base and collector currents and record them in the first row of Table 20.5.3 (Theory). As the circuit is in saturation, the theoretical V_{CE} is close to zero and may be found on the transistor data sheet via the V_{CE}/I_C saturation graph. Record this value in the first row of Table 20.5.3 as well.

7. Build the saturating switch of Figure 20.3.2 using Vee = Vbb = 5 volts, Rb = 4.7 kΩ and Rc = 220 Ω. Measure and record the base and collector currents, and record the collector-emitter voltage in the first row of Table 20.5.3 (Experimental). Also compute and record the deviations between theory and experimental results.

8. Remove the base resistor from Vbb and connect it to ground. Without a base source potential, the circuit will be in cutoff. Determine the theoretical base and collector currents along with the collector-emitter voltage and record them in the second row of Table 20.5.3. Measure these parameters, record them in Table 20.5.3, and also compute and record the resulting deviations.

9. Reconnect the base resistor to the Vbb supply and swap in the second transistor. Repeat steps 3 and 4 using the next two rows of Table 20.5.3.

10. Reconnect the base resistor to the Vbb supply and swap in the third transistor. Repeat steps 3 and 4 using the final two rows of Table 20.5.3.

8.5.4.4 20.4.4: Design

11. A simple way to program the LED current in the driver is by altering the collector resistor. First, measure the LED potential while it is lit. Assuming that the collector-emitter saturation voltage is negligible, all of the power supply voltage will drop across the collector resistor when the LED is lit, with the exception of the LED voltage. Ohm's law can then be used to determine a resistance value for a desired target current. Compute the required value of resistance to achieve an LED current of 8 mA. Replace the collector resistor with the nearest value available and measure the resulting current. Record the appropriate values in Table 20.5.4.

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8.5.5: Data Tables

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$
1						
2						
3						

Table 8.5.5.1

Issue	V_B	V_E	V_C
R_2 Short			
R_e Open			
R_C Short			
R_C Open			
V_{CE} Short			
V_{CE} Open			

Table 8.5.5.2

Vbb	$I_{B\ Theory}$	$I_{C\ Theory}$	$V_{CE\ Theory}$	$I_{B\ Exp}$	$I_{C\ Exp}$	$V_{CE\ Exp}$
5						
0						
5						
0						
5						
0						

Table 8.5.5.3

$R_{C\ Theory}$	$R_{C\ Actual}$	$I_{C\ Measured}$

Table 8.5.5.4

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8.5.6: Questions

1. Is the PNP voltage divider circuit as stable as its NPN counterpart studied earlier?

2. Compare the NPN voltage divider lab results to this PNP version. If the various transistor voltages are added together (e.g., NPN base voltage plus PNP base voltage), a constant results. What is the significance of this value and will it always work out in this fashion? Why/why not?

3. Do the troubleshooting faults presented in the PNP circuit produce similar transistor voltages compared to the same faults in the NPN version of the circuit? Why/why not?

4. How does the operational logic of the PNP LED driver compare to the NPN version of the same circuit?

5. Are the LED current design considerations the same as those of the NPN version?

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SECTION OVERVIEW

8.6: Common Emitter Amplifier

Objective

The objective of this exercise is to examine the characteristics of a common emitter amplifier, specifically voltage gain, input impedance and output impedance. A method for experimentally determining input and output impedance is investigated along with various potential troubleshooting issues.

8.6.1: Theory Overview

8.6.2: Equipment

8.6.3: Schematics

8.6.4: Procedure

8.6.5: Data Tables

8.6.6: Questions

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8.6.1: Theory Overview

An ideal common emitter amplifier simply multiples the input function by a constant value while also inverting the signal. The voltage amplification factor, A_v, is largely a function of the AC load resistance at the collector and the internal emitter resistance, r'_e. This internal resistance is, in turn, inversely proportional to the DC emitter current. Therefore, if the underlying bias is stable with changes in beta, the voltage gain will also be stable. The circuit will appear as an impedance to the signal source, Z_{in}. This impedance is approximately equal to the base biasing resistor(s) in parallel with the impedance seen looking into the base $(Z_{in(base)})$ which is approximately equal to $\beta\, r'_e$. Consequently, the amplifier's input impedance may experience some variation with beta. In contrast, the circuit's output impedance as seen by the load is approximately equal to the DC collector biasing resistor.

From a practical standpoint, input and output impedance cannot be measured directly with an ohmmeter. This is because ohmmeters measure resistance by sending out a small "sensing" current. The DC bias and AC signal currents will interact with this current and produce an unreliable result. Instead, impedances can be measured indirectly through a voltage divider effect. That is, if the voltages of both legs of a voltage divider can be measured and the resistance of one of the legs is known, the remaining resistance may be determined using Ohm's law or the voltage divider rule.

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8.6.2: Equipment

(1) Dual adjustable DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

(1) Dual channel oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(3) Small signal transistors (2N3904)

(1) 10 k Ω resistor 1/4 watt

actual: _____

(1) 15 k Ω resistor 1/4 watt

actual: _____

(1) 20 k Ω resistor 1/4 watt

actual: _____

(1) 22 k Ω resistor 1/4 watt

actual: _____

(1) 33 k Ω resistor 1/4 watt

actual: _____

(2) 10 μF capacitors

actual: _____

(1) 470 μF capacitor

actual: _____

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8.6.3: Schematics

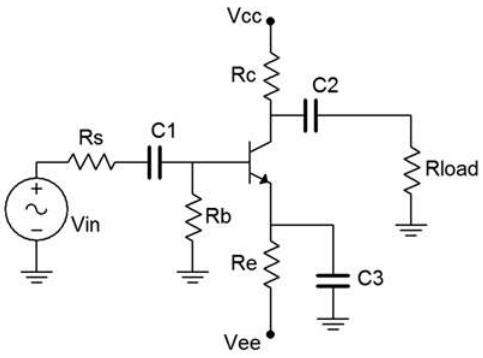


Figure 8.6.3.1

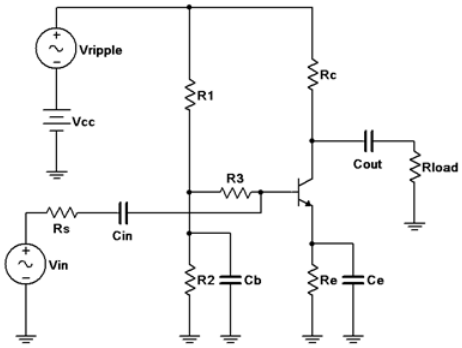


Figure 8.6.3.2

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8.6.4: Procedure

8.6.4.1 21.4.1: DC Circuit Voltages

1. Consider the circuit of Figure 21.3.1 using Vcc = 15 volts, Vee = −12 volts, Rs = 10 kΩ, Rb = 33 kΩ, Re = 22 kΩ, Rc = 15 kΩ, Rload = 20 kΩ, C1 = C2 = 10 μF and C3 = 470 μF. Using the approximation of a negligible base voltage, determine the DC voltages at the base, emitter, and collector along with the collector current, and record these in Table 21.5.1.

2. Build the circuit of Figure 21.3.1 using Vcc = 15 volts, Vee = −12 volts, Rs = 10 kΩ, Rb = 33 kΩ, Re = 22 kΩ, Rc = 15 kΩ, Rload = 20 kΩ, C1 = C2 = 10 μF and C3 = 470 μF. Make sure that the AC source is turned off or disconnected. Measure the DC voltages at the base, emitter, and collector along with the collector current, and record these in Table 21.5.1. Note, you may wish to use a transistor curve tracer or beta checker to get approximate values of beta for each of the three transistors to be used.

8.6.4.2 21.4.2: AC Circuit Voltages

3. Based on the calculated collector current, determine the resulting theoretical r'_e, A_v, Z_{in} and Z_{out}, and record these in Table 21.5.2. Assume a beta of approximately 150 for the Z_{in} calculation.

4. Continuing with the values in Table 21.5.2 and using an AC source voltage of a 40 mV peak-peak 1 kHz sine wave, compute the theoretical AC base, emitter and load voltages, and record them in Table 21.5.3 (Theory). Note that R_s will create a voltage divider effect with Z_{in}, thus reducing the signal that reaches the base. This reduced signal is then multiplied by the voltage gain and appears at the collector.

5. Set the source to a 40 mV peak-peak 1 kHz sine wave and apply to the circuit. Using the oscilloscope, place one probe at the base and the second at the emitter. Record the resulting peak-peak voltages in the first row of Table 21.5.3 (Experimental). The oscilloscope inputs should be set for AC coupling with the bandwidth limit engaged. Capture an image of the oscilloscope display.

6. Move the second probe to the load and record its peak-peak value in the first row of Table 21.5.3. Also include whether the signal is in phase or out of phase with the base signal. Capture an image of the oscilloscope display.

7. Unhook the load resistor from the output capacitor and measure the resulting collector voltage (do not connect the output capacitor to ground-simply leave it dangling). Record this value in the final column of Table 21.5.3.

8. Reattach the load resistor. Swap the transistor with the second transistor and repeat steps 5 through 7 using the second row of Table 21.5.3.

9. Reattach the load resistor. Swap the transistor with the third transistor and repeat steps 5 through 7 using the third row of Table 21.5.3.

10. Using the measured base and collector voltages from Table 21.5.3, determine the experimental gain for each transistor. From these gains determine the experimental r'_e. Using the source voltage, the measured base voltages and the source resistance, determine the effective input impedances via Ohm's law or the voltage divider rule. Finally, in similar manner and using the loaded and unloaded collector voltages along with the load resistor value, determine the experimental output impedances. Record these values in Table 21.5.4. Also determine and record the percent deviations.

8.6.4.3 21.4.3: Troubleshooting

11. Return the load resistor to the circuit. Consider each of the individual faults listed in Table 21.5.5 and estimate the resulting AC load voltage. Introduce each of the individual faults in turn and measure and record the load voltage in Table 21.5.5.

8.6.4.4 21.4.4: Computer Simulation

12. One issue with amplifiers is noise and ripple on the power supply. This will be directly coupled to output of the circuit via the collector resistor. Worse, this noise or ripple may be coupled into the base and then amplified along with the desired input signal. This can be an issue with amplifiers that use a voltage divider bias. One way to reduce this effect is to decouple the voltage divider from the base. This modification is shown in the circuit of Figure 21.3.2. Cb effectively shorts R2, sending power supply noise and ripple to ground instead of into the base. By itself this would also short the desired input signal so an extra resistor, R3 is added between the capacitor and the base. The input impedance of the circuit is approximately equal to R3 in parallel with $\beta\, r'_e$. To show

the effectiveness of this technique, build the circuit of Figure 21.3.2 in a simulator. Use values of Vin = 20 mV peak at 1 kHz, Vripple = 20 mV peak at 120 Hz, Vcc = 12 volts, Rs = 1 kΩ, R1 = 10 kΩ, R2 = 3.3 kΩ, R3 = 22 kΩ, Re = 4.7 kΩ, Rc = 3.3 kΩ, Rload = 1 kΩ, Cin = Cout = 10 μF, Cb= 100 μF and Ce = 470 10 μF. Run a Transient simulation and look at the load voltage. A very small low frequency variation should be noted. This is the 120 Hz ripple coupled in through the collector resistor. Alter the circuit by removing Cb and R3 to produce the basic voltage divider circuit (or more simply, set Cb and R3 to extremely small values such as pF and mΩ). Rerun the simulation. The load voltage should now show a much more obvious ripple contribution, thus showing how effective the power supply decoupling components can be.

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8.6.5: Data Tables

$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{C\ Thry}$	$I_{C\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{C\ Exp}$	$I_{C\ Exp}$

Table 8.6.5.1

r'_e	A_v	Z_{in}	Z_{out}

Table 8.6.5.2

Transistor	$V_{B\ Thry}$	$V_{E\ Thry}$	$V_{L\ Thry}$	$V_{B\ Exp}$	$V_{E\ Exp}$	$V_{L\ Exp}$	Phase V_L	$V_{L\ No\ Load}$
1								
2								
3								

Table 8.6.5.3

Transistor	$A_{v\ Exp}$	$r'_{e\ Exp}$	$Z_{in\ Exp}$	$Z_{out\ Exp}$	%D A_v	%D r'_e	%D Z_{in}	%D Z_{out}
1								
2								
3								

Table 8.6.5.4

Issue	V_{Load}
R_B Short	
C_1 Open	
R_C Short	
R_C Open	
R_E Open	
C_2 Open	
C_3 Open	
V_{CE} Open	

Table 8.6.5.5

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8.6.6: Questions

1. Does the common emitter amplifier produce a considerable amplification effect and if so, are the results consistent across transistors?

2. Does the common emitter amplifier produce a phase shift at the output and if so, is it affected by the transistor beta?

3. If the collector and base voltages had been measured with the oscilloscope DC coupled, how would the measurements of Table 21.5.3 have changed?

4. Does the value of the transistor beta play any role in setting the input impedance? Was a considerable variation in input impedance apparent?

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9.5.2: Reference

9.5.3: Equipment
9.5.4: Components
9.5.5: Schematics
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SECTION OVERVIEW

9.1: Decibels and Bode Plots

Objective

In this exercise, the usage of decibel measurements and Bode plots will be examined. The investigation will include the relationship between ordinary and decibel gain, and the decibel-amplitude and phase response of a simple lag network.

9.1.1: Theory Overview

9.1.2: Reference

9.1.3: Equipment

9.1.4: Components

9.1.5: Schematics

9.1.6: Procedure

9.1.7: Data Tables

9.1.8: Questions

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9.1.1: Theory Overview

The decibel is a logarithmic-based measurement scheme. It is based on ratios of change. Positive values indicate an increase while negative values indicate a decrease. Decibel schemes can be used for gains and, with minor modification, signal levels. A Bode plot shows the variations of gain (typically expressed in decibels) and phase across a range of frequencies for some particular circuit. These will prove to be very valuable in later design and analysis work.

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9.1.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 1.2, The Decibel

Section 1.3, Bode Plots

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9.1.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Decibel-reading voltmeter

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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9.1.4: Components

(1) 100n F

actual:_____

(1) 100 Ω

actual:_____

(1) 1k Ω

actual:_____

(1) 4k7 Ω

actual:_____

(2) 10k Ω

actual:_____ _____

(1) 22k Ω

actual:_____

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9.1.5: Schematics

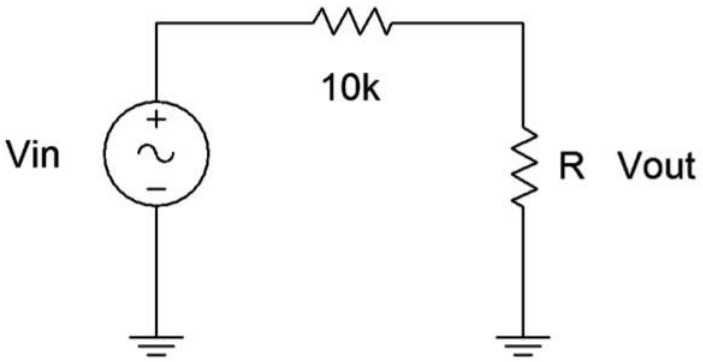


Figure 9.1.5.1

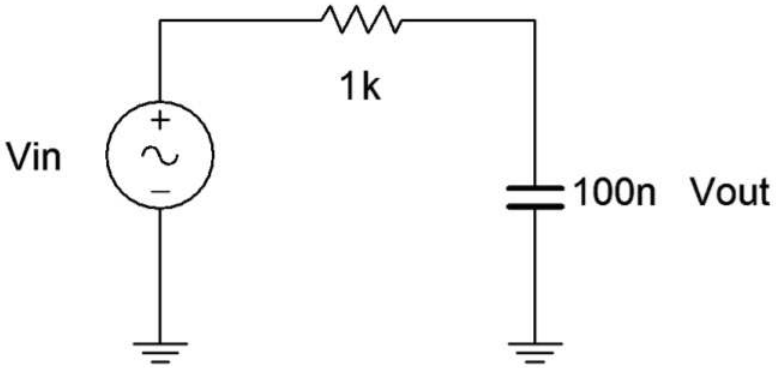


Figure 9.1.5.2

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9.1.6: Procedure

1. Calculate the voltage gains (losses) for the voltage divider of Figure 1.5.1 for the resistor values specified, and record them in Table 1.7.1. Also, convert each of the ordinary gains into decibel form.

2. Assemble the circuit of Figure 1.5.1 using the 22k resistor.

3. Set the generator to a 100 Hz sine wave, 0 dBV (Note: If the meter is calibrated in dBu, then use 0 dBu).

4. Apply the generator to the circuit. Measure and record the output voltage in Table 1.7.1 using the decibel-reading voltmeter. Also, compute the resulting experimental decibel voltage gain and gain deviation.

5. Repeat step 4 for the remaining resistor values in Table 1.7.1.

6. To create a simple Bode plot, the lag network of Figure 1.5.2 will be used. Assemble this circuit and record its theoretical critical frequency in Table 1.7.2.

7. Set the generator to a 1 kHz sine wave, 0 dBV.

8. Apply the generator to the circuit. Determine the experimental critical frequency by adjusting the frequency of the generator until the circuit's output voltage is –3 dBV. Record the measured frequency in Table 1.7.2.

9. Set the generator to a sine wave at one-tenth of the experimental critical frequency.

10. Adjust the generator's output level to 0 dBV.

11. Apply the generator to the circuit. Measure and record the output level in decibels in Table 1.7.3. Also, measure and record the phase angle between the input and output waveforms and record it in Table 1.7.3.

12. Repeat steps 9 through 11 for the remaining frequencies listed in Table 1.7.3.

13. Using the values from Table 1.7.3, create a Bode plot for this circuit using a log scaled horizontal axis (i.e., semi-log paper).

9.1.6.1 1.6.1: Computer Simulation

14. Build the lag network of Figure 1.5.2 in a simulator and run an AC Analysis. Be sure to run this from at least one decade below the critical frequency to at least one decade above. Also, use a decibel scale for the gain amplitude. Compare the results to the Bode plot generated in Step 13 and include this graph with the technical report.

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9.1.7: Data Tables

R	A_v Theory	A_v' Theory	V_{out}'	Experimental A_v'	% Deviation
22k Ω					
10k Ω					
4k7 Ω					
1k Ω					
100 Ω					

Table 9.1.7.1

Theoretical f_c	
Experimental f_c	

Table 9.1.7.2

Factor	Frequency	A_v'	Phase
.1 f_c			
.2 f_c			
.5 f_c			
f_c			
2 f_c			
5 f_c			
10 f_c			

Table 9.1.7.3

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9.1.8: Questions

1. Is the logarithmic nature of the decibel apparent in the data of Table 1.7.1?

2. Using the plot created in step 13, determine the slope in dB-per-octave in the region above f_c.

3. What would the plot of step 13 look like if ordinary gains had been used instead of decibel gains?

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SECTION OVERVIEW

9.2: The Differential Amplifier

Objective

In this exercise, the performance of a differential amplifier will be examined. The investigation will include the DC parameters of input bias and offset current, and output offset voltage. The AC parameters of interest are the differential and common-mode gains, and the resulting common-mode rejection-ratio (CMRR).

9.2.1: Theory Overview

9.2.2: Reference

9.2.3: Equipment

9.2.4: Components

9.2.5: Schematics

9.2.6: Procedure

9.2.7: Data Tables

9.2.8: Questions

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9.2.1: Theory Overview

The ideal differential amplifier is perfectly symmetrical producing identical DC input bias currents and output collector voltages. Several factors ranging from the mismatch of transistor parameters to resistor tolerances prevent perfect symmetry in a practical circuit. The DC quality of the circuit can be expressed in terms of the mismatches. The difference between the input bias currents is known as the input offset current. The difference between the output collector voltages is known as the output offset voltage. For AC performance, the primary items of concern are the differential and common-mode gains. The ideal differential amplifier will only amplify differential input signals, and thus, has a common-mode gain of zero. Due to component mismatches and internal design limits, the common-mode gain is never zero, allowing some portion of the common-mode input signal to make its way to the output. The measure of the suppression of common-mode signals is given by the common-mode rejection-ratio, or CMRR. CMRR can be found by dividing the differential gain by the common-mode gain.

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9.2.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 1.6, The Differential Amplifier

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9.2.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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9.2.4: Components

(3) Small signal NPN transistors (2N3904, 2N2222, etc.)

(2) 100 Ω

actual:_____ _____

(2) 330 Ω

actual:_____ _____

(2) 470 Ω

actual:_____ _____

(1) 3k3 Ω

actual:_____

(2) 4k7 Ω

actual:_____ _____

(1) 5k6 Ω

actual:_____

(1) 10k Ω

actual:_____

(2) 22k Ω

actual:_____ _____

(1) 33k Ω

actual:_____

2N3904 Datasheet: https://www.onsemi.com/pub/Collateral/2N3903-D.PDF

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9.2.5: Schematics

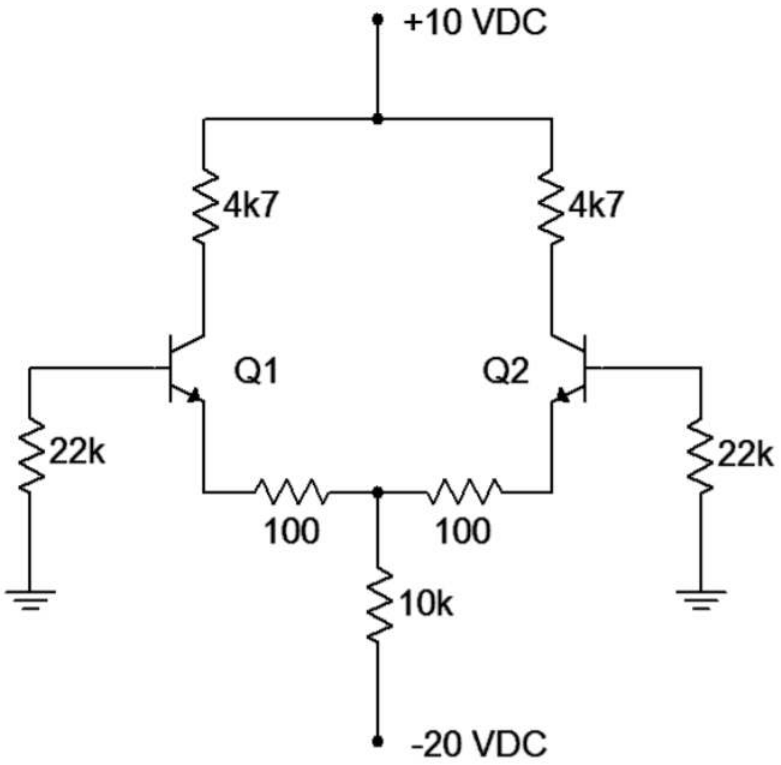


Figure 9.2.5.1

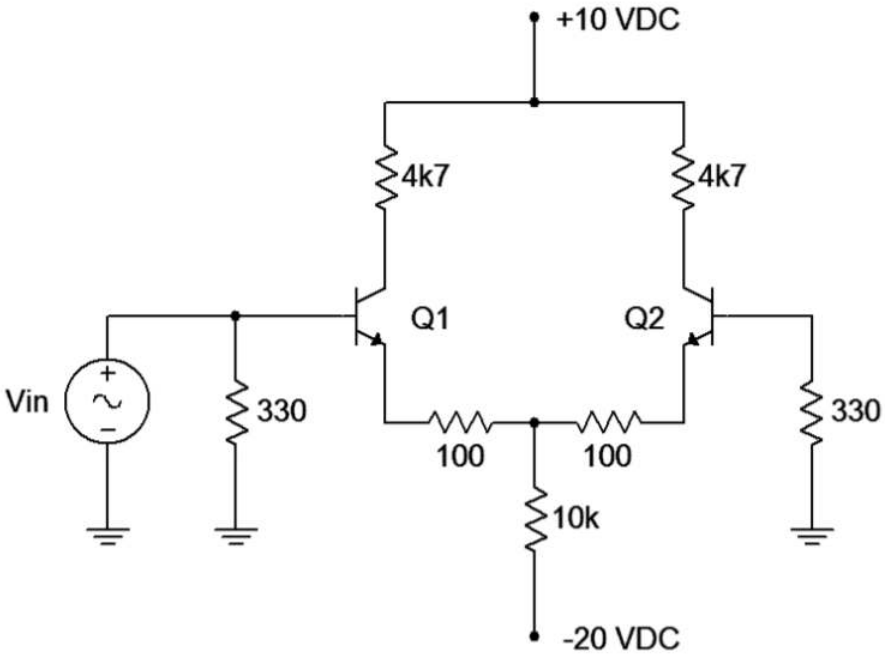


Figure 9.2.5.2

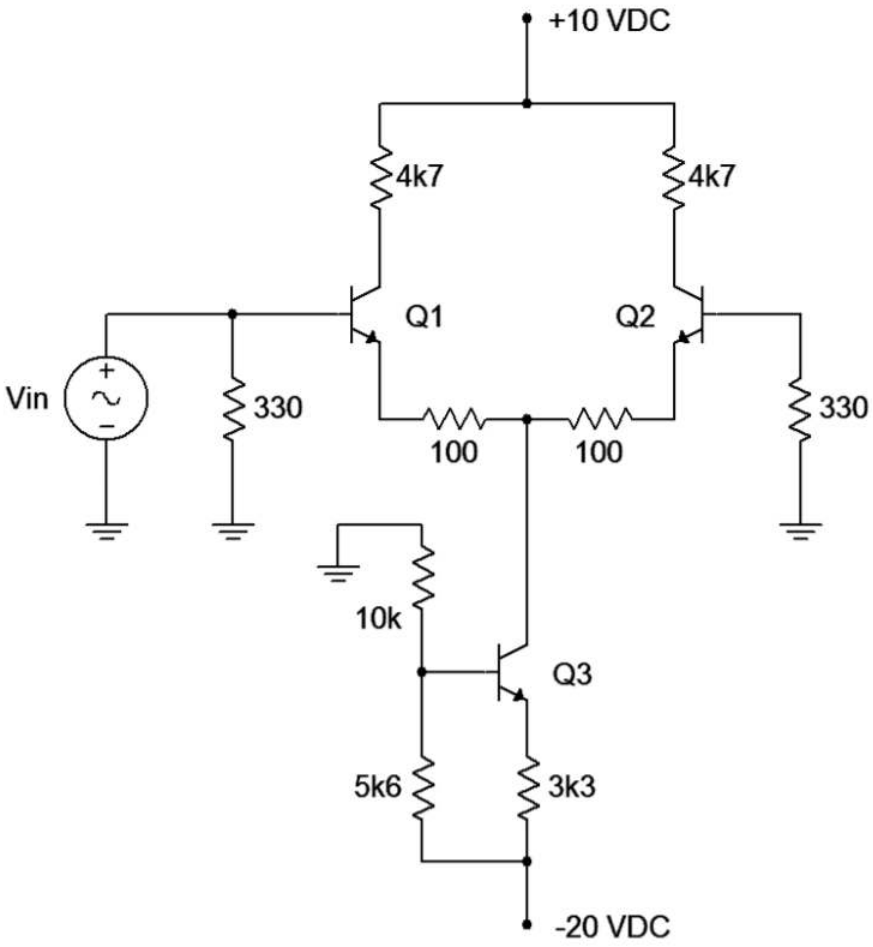


Figure 9.2.5.3

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9.2.6: Procedure

9.2.6.1 2.6.1: DC Parameters

1. Assume that the transistors of Figure 2.5.1 have a current gain of 150. Calculate the base currents and collector voltages for the amplifier of Figure 2.5.1 and record them in Table 2.7.1. Also, compute and record the theoretical (ideal) input offset current and output offset voltage.

2. Assemble the circuit of Figure 2.5.1.

3. Measure and record the base currents in Table 2.7.1. (Note: You may wish to measure the voltage across the base resistors and compute the base currents if the DMM cannot measure small DC currents.) Based on these currents, compute and record the experimental input bias and offset currents along with the corresponding deviations.

4. Measure and record the collector voltages in Table 2.7.1. Based on these voltages, compute and record the experimental output offset voltage and the corresponding deviation.

9.2.6.2 2.6.2: AC Parameters

5. Calculate the differential voltage gain and collector voltages for the amplifier of Figure 2.5.2 using an input of 20 millivolts, and record them in Table 2.7.2.

6. Assemble the circuit of Figure 2.5.2.

7. Set the generator to a 1 kHz sine wave, 20 millivolts peak.

8. Apply the generator to the amplifier. Measure and record the AC collector voltages in Table 2.7.2 while noting the phase relative to the input. Also, compute the resulting experimental voltage gain from the input to collector one, and the deviations.

9. Apply the generator to both inputs. Set the generator's output to 1 volt peak.

10. Measure the AC voltage at collector one and record it in Table 2.7.3.

11. Based on the value measured in step 10, compute and record the common-mode gain and CMRR in Table 2.7.3.

9.2.6.3 2.6.3: Improved CMRR

12. Assemble the circuit of Figure 2.5.3. This circuit uses an improved tail current source that exhibits much higher internal impedance than the circuit of Figure 2.5.2. This should yield a decrease in common mode gain which, in turn, should yield an improved CMRR. Note that the new circuit sets up virtually the same tail current, therefore producing approximately the same DC parameters and differential gain as the original.

13. Repeat steps 9 through 11 recording the results in Table 2.7.4.

9.2.6.4 2.6.4: Troubleshooting

14. Continuing with the amplifier of Figure 2.5.3, turn the signal down to 0. Estimate and then measure the results for each individual error presented in Table 2.7.5.

9.2.6.5 2.6.5: Computer Simulation

15. Build the amplifier of Figure 2.5.2 in a simulator and run a Transient Analysis echoing steps 5 through 8. Compare the results to the data found in Table 2.7.2.

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9.2.7: Data Tables

DC Quantity	Theoretical	Experimental	% Deviation
I_{B1}			
I_{B2}			
$I_{in-bias}$			
$I_{in-offset}$			n/a
V_{C1}			
V_{C2}			
$V_{out-offset}$			n/a

Table 9.2.7.1

AC Quantity	Theoretical	Experimental	% Deviation
V_{C1}			
V_{C2}			
A_v			

Table 9.2.7.2

V_{C1}	
A_{cm}	
CMRR	

Table 9.2.7.3

V_{C1}	
A_{cm}	
CMRR	

Table 9.2.7.4

Error	Quantity	Estimate	Actual
3k3 is replaced with 33k	V_{C1} DC		
Q_1's 4k7 is 470	V_{C1} DC		
Both 4k7 are 470	V_{C1} DC		

Table 9.2.7.5

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9.2.8: Questions

1. How might the input offset current of Figure 2.5.1 be reduced?

2. What are some causes of output offset voltage in the circuit of Figure 2.5.1?

3. What are the effects if the two collector resistors not identical in value?

4. What is the significance of a high CMRR?

5. How significant is the change in CMRR when using the improved current source? Based on the improvement, estimate the internal impedance of the current source.

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SECTION OVERVIEW

9.3: The Non-inverting Voltage Amplifier

Objective

In this exercise, the performance of the non-inverting voltage amplifier will be examined. The investigation will include the effect of feedback resistors on setting voltage gain, stability of gain with differing op amps, and input impedance.

9.3.1: Theory Overview

9.3.2: Reference

9.3.3: Equipment

9.3.4: Components

9.3.5: Schematics

9.3.6: Procedure

9.3.7: Data Tables

9.3.8: Questions

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9.3.1: Theory Overview

The non-inverting voltage amplifier is based on series-parallel negative feedback. As the ideal voltage-controlled voltage source, this amplifier exhibits high input impedance, low output impedance, and stable voltage gain. The voltage gain is set by the two feedback resistors, R_i and R_f.

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9.3.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 3.4, The Four Variants of Negative Feedback

Section 4.2, Inverting and Non-inverting Amplifiers

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9.3.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

9.3.3.1 4.3.1: For Distortion Measurement Only

(1) Low distortion sine source

model:_____ srn:_____

(1) Distortion analyzer

model:_____ srn:_____

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9.3.4: Components

(3) General purpose op amps (1 each of 741, 351, 318, 411, 081, etc.)

(2) 1μ F

actual:_____ _____

(1) 1k Ω

actual:_____

(1) 4k7 Ω

actual:_____

(1) 10k Ω

actual:_____

(1) 22k Ω

actual:_____

(1) 33k Ω

actual:_____

(1) 47k Ω

actual:_____

(1) 100k Ω

actual:_____

LM741 Datasheet: http://www.ti.com/lit/ds/symlink/lm741.pdf

LF351 Datasheet: https://www.st.com/resource/en/datasheet/lf351.pdf

LF411 Datasheet: http://www.ti.com/lit/ds/symlink/lf411.pdf

LM318 Datasheet: http://www.ti.com/lit/ds/symlink/lm318-n.pdf

TL081 Datasheet: http://www.ti.com/lit/ds/symlink/tl081.pdf

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9.3.5: Schematics

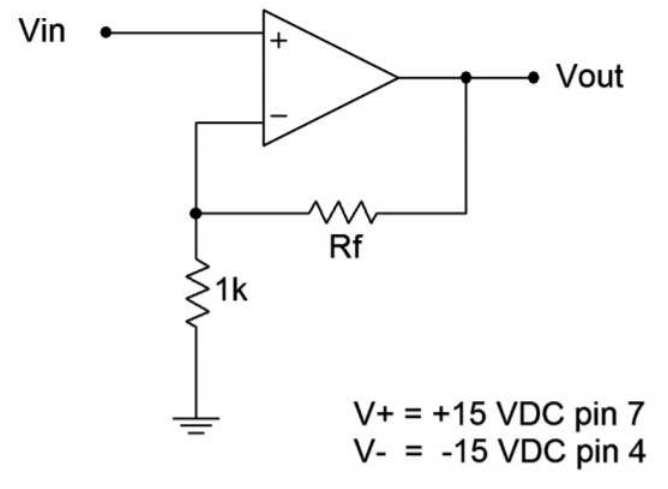


Figure 9.3.5.1

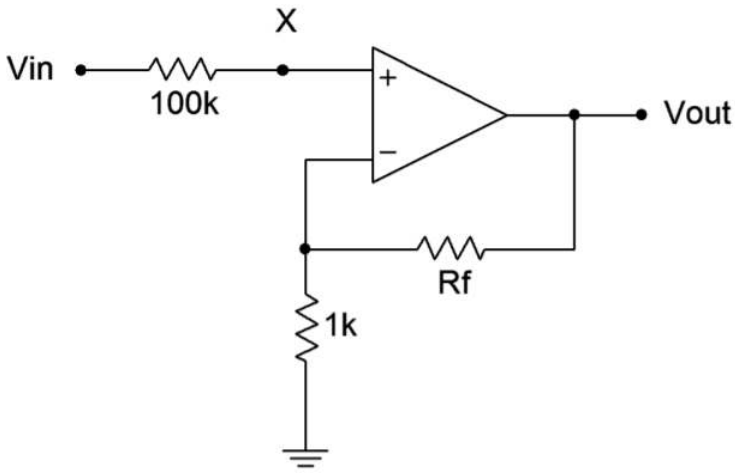


Figure 9.3.5.2

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9.3.6: Procedure

1. The voltage gain of the non-inverting amplifier can be determined accurately from the feedback resistors R_i and R_f. Calculate the voltage gains for the amplifier of Figure 4.5.1 for the R_f values specified, and record them in Table 4.7.1.

2. Assemble the circuit of Figure 4.5.1 using the 4k7 Ω resistor.

3. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

4. Apply the generator to the amplifier. Measure and record the output voltage in Table 4.7.1. Also, compute the resulting experimental voltage gain and gain deviation.

5. Repeat step 4 for the remaining R_f values in Table 4.7.1.

6. For any given R_i, R_f combination, the voltage gain should be stable regardless of the precise op amp used, even if it is of an entirely different model. To verify this, first set R_f to 22k Ω.

7. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

8. Apply the generator to the amplifier. Measure and record the output voltage in Table 4.7.2. Also, compute the resulting experimental voltage gain and gain deviation.

9. Repeat step 8 for two other op amps.

10. It is not practical to use an ohmmeter to determine the input impedance of an active circuit. Instead, input impedance can be found by utilizing the voltage divider effect. Modify the circuit by adding the extra input resistor as shown in Figure 4.5.2.

11. Set R_f to 4k7 Ω.

12. Set the generator to a 200 Hz sine wave, 1 volt peak.

13. Apply the generator to the amplifier. Use a DMM to measure and record the AC potential from V_{in} to point X (i.e.,V_A, the voltage across the 100k) in Table 4.7.3. Using KVL, determine the voltage from point X to ground (V_B) and record in Table 4.7.3 (don't forget to compensate for peak versus RMS readings). Finally, compute the resulting input impedance by using the voltage divider rule. Note: If the DMM is not sensitive enough and registers 0 volts for V_A, it is safe to assume that Z_{in} is considerably larger than the 100k Ω sensing resistor.

9.3.6.1 4.6.1: Distortion Measurement

14. Return to the amplifier of Figure 4.5.1 with R_f set to 10k Ω. If available, the LF351 is a good choice for the op amp in this portion. Replace the general purpose generator with the low distortion sine source set to 1 kHz. Adjust its output level so that the output of the op amp is approximately 0 dBV.

15. Apply the distortion analyzer to the output of the op amp, read the resulting THD percentage and record it in Table 4.7.4.

16. Repeat steps 14 and 15 using the remaining R_f values in Table 4.7.4.

9.3.6.2 4.6.2: Troubleshooting

17. Continuing with the amplifier of Figure 4.5.1, reset R_f to 4k7 Ω. Estimate and then measure the results for each individual error presented in Table 4.7.5.

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9.3.7: Data Tables

R_f	Theoretical A_v	V_{out}	Experimental A_v	% Deviation
4k7 Ω				
10k Ω				
22k Ω				
33k Ω				
47k Ω				

Table 9.3.7.1

Op Amp	Theoretical A_v	V_{out}	Experimental A_v	% Deviation
1				
2				
3				

Table 9.3.7.2

V_A	V_B	Z_{in}

Table 9.3.7.3

R_f	% THD
10k Ω	
22k Ω	
47k Ω	

Table 9.3.7.4

Error	Quantity	Estimate	Actual
R_i's third band is orange	V_{out}		
f_{in} is 100 Hz	V_{out}		
R_i is swapped with R_f	V_{out}		
+ and – signal input pins swapped	V_{out}		

Table 9.3.7.5

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9.3.8: Questions

1. What is the effect as R_f is increased?

2. How does the voltage gain vary as the op amp is changed?

3. Does the non-inverting voltage amplifier exhibit a predictable and stable voltage gain?

4. What can be said about the input impedance of this type of amplifier?

5. What is the relationship between gain, feedback and distortion?

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SECTION OVERVIEW

9.4: The Inverting Voltage Amplifier

Objective

In this exercise, the performance of the inverting voltage amplifier will be examined. The investigation will include the effect of feedback resistors on setting voltage gain, stability of gain with differing op amps, and the concept of virtual ground.

9.4.1: Theory Overview

9.4.2: Reference

9.4.3: Equipment

9.4.4: Components

9.4.5: Schematics

9.4.6: Procedure

9.4.7: Data Tables

9.4.8: Questions

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9.4.1: Theory Overview

The inverting voltage amplifier is based on parallel-parallel negative feedback. This amplifier exhibits modest input impedance, low output impedance, and stable inverting voltage gain. The voltage gain is set by the two feedback resistors, R_i and R_f.

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9.4.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 4.2, Inverting and Non-inverting Amplifiers

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9.4.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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9.4.4: Components

(3) General purpose op amps (1 each of 741, 351, 318, 411, 081, etc.)

(2) 1μ F

actual:_____ _____

(1) 1k Ω

actual:_____

(1) 4k7 Ω

actual:_____

(1) 10k Ω

actual:_____

(1) 22k Ω

actual:_____

(1) 33k Ω

actual:_____

(1) 47k Ω

actual:_____

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9.4.5: Schematics

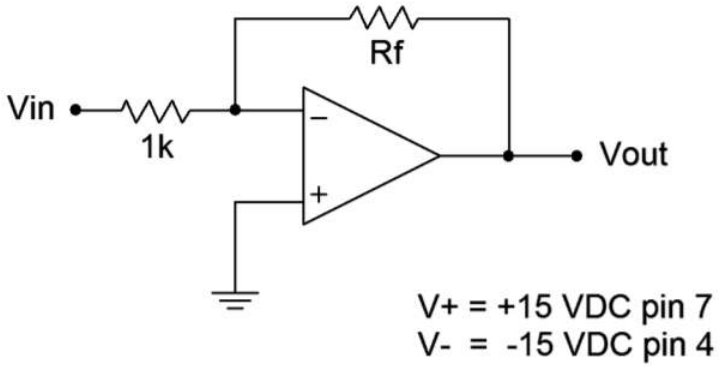


Figure 9.4.5.1

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9.4.6: Procedure

1. The voltage gain of the inverting amplifier can be determined accurately from the feedback resistors R_i and R_f. Calculate the voltage gains for the amplifier of Figure 5.5.1 for the R_f values specified, and record them in Table 5.7.1.

2. Assemble the circuit of Figure 5.5.1 using the 4k7 Ω resistor.

3. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

4. Apply the generator to the amplifier. Measure and record the output voltage in Table 5.7.1, noting its phase relative to the input. Also, compute the resulting experimental voltage gain and gain deviation.

5. Repeat step 4 for the remaining R_f values in Table 5.7.1.

6. For any given R_i, R_f combination, the voltage gain should be stable regardless of the precise op amp used, even if it is of an entirely different model. To verify this, first set R_f to 22k Ω.

7. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

8. Apply the generator to the amplifier. Measure and record the output voltage in Table 5.7.2. Also, compute the resulting experimental voltage gain and gain deviation.

9. Repeat step 8 for two other op amps.

10. The concept of virtual ground is very important. A virtual ground exists at the inverting input of the op amp in this circuit. Ideally, the voltage at this point should be very close to 0. Through voltage divider effect, this implies that all of the input signal must be dropping across R_i, and thus R_i must establish the input impedance of the amplifier.

11. Set R_f to 4k7 Ω.

12. Set the generator to a 200 Hz sine wave, 1 volt peak.

13. Apply the generator to the amplifier. Use a DMM to measure and record the AC potential at the inverting terminal of the op amp. Record the value in Table 5.7.3.

9.4.6.1 5.6.1: Computer Simulation

14. Build the circuit in a simulator and run a Transient Analysis echoing steps 2 through 5. Compare the results to the waveforms generated experimentally.

15. Repeat step 14 but this time use the Distortion Analyzer instrument to compare voltage gain to THD.

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9.4.7: Data Tables

R_f	A_v Theory	V_{out}'	Phase	Experimental A_v	% Deviation
4k7 Ω					
10k Ω					
22k Ω					
33k Ω					
47k Ω					

Table 9.4.7.1

Op Amp	A_v Theory	V_{out}	Experimental A_v	% Deviation
1				
2				
3				

Table 9.4.7.2

V_{inverting-input}\)	

Table 9.4.7.3

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9.4.8: Questions

1. What is the effect as R_f is increased?

2. How does the voltage gain vary as the op amp is changed?

3. Does the inverting voltage amplifier exhibit a predictable and stable voltage gain?

4. What can be said about the input impedance of this type of amplifier?

5. Based on the simulation, what is the relationship between gain, feedback and distortion for this circuit?

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SECTION OVERVIEW

9.5: The Op Amp Differential Amplifier

Objective

In this exercise, the performance of an op amp based differential amplifier will be examined. The investigation will include the effects of differential gain and common-mode rejection ratio (CMRR).

9.5.1: Theory Overview

9.5.2: Reference

9.5.3: Equipment

9.5.4: Components

9.5.5: Schematics

9.5.6: Procedure

9.5.7: Data Tables

9.5.8: Questions

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9.5.1: Theory Overview

An op amp differential amplifier can be created by combining both a non-inverting voltage amplifier and an inverting voltage amplifier in a single stage. Proper gain matching between the two paths is essential to maximize the common-mode rejection ratio. Differential gain is equal to the gain of the inverting path.

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9.5.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

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9.5.3: Equipment

(1) Oscilloscope

model:_____ srn:_____

(1) Function generator

model:_____ srn:_____

(1) Dual DC power supply

model:_____ srn:_____

(1) DMM

model:_____ srn:_____

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9.5.4: Components

(2) General purpose op amps (741, 351, etc.)

(2) 1 μF

actual:_____ _____

(2) 10 kΩ

actual:_____ _____

(1) 15 kΩ

actual:_____

(1) 22 kΩ

actual:_____

(2) 100 kΩ

actual:_____ _____

(1) 10 kΩ potentiometer

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9.5.5: Schematics

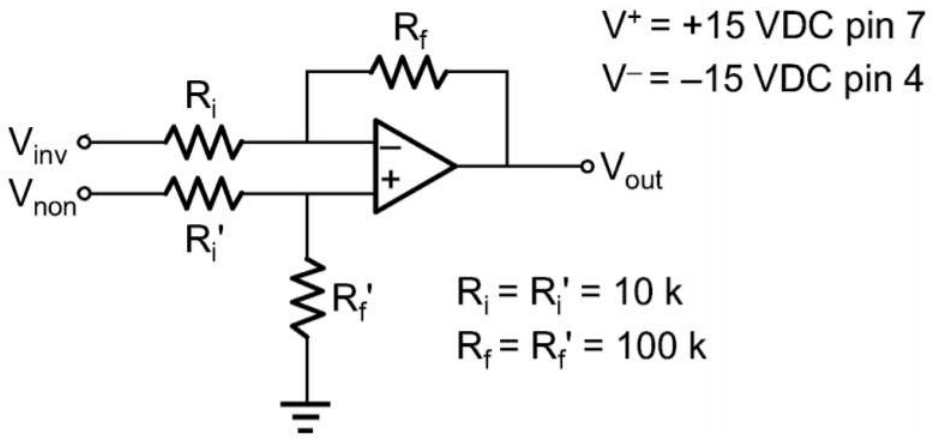


Figure 9.5.5.1

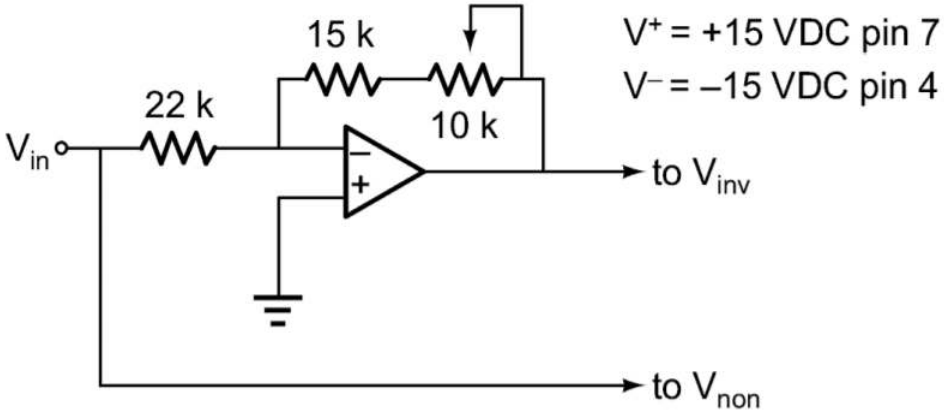


Figure 9.5.5.2

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9.5.6: Procedure

1. This circuit can be examined through the use of the Superposition Theorem. The contribution of each input can be measured individually, combined, and then compared with common-mode and differential inputs.

2. Calculate the differential voltage gain for the amplifier and record it in Table 6.7.1

3. Assemble the circuit of Figure 6.5.1. Try to get the R_i/R_f ratio as close as possible to the R_i'/R_f' ratio, even if you have to mix and match several resistors.

4. Set the generator to a 1 kHz sine wave, 500 millivolts peak.

5. Apply the generator to the V_{inv} input, and ground the V_{non} input.

6. Measure and record the output voltage in Table 6.7.2, noting the phase relative to the input. Also, compute the resulting voltage gain.

7. Swap the inputs by connecting the V_{non} input to the generator, and grounding the V_{inv} input.

8. Measure and record the output voltage in Table 6.7.2, noting the phase relative to the input. Also, compute the resulting voltage gain.

9. Compare the results of step 6 to step 8. The gains should be identical except that one is inverting while the other is non-inverting. Calculate the results of adding the two output signals and place the values in Table 6.7.3.

10. To measure the common-mode gain, connect both inputs to the generator (removing the V_{inv} ground). Record the output voltage and resulting gain in Table 6.7.3.

11. Assemble the circuit of Figure 6.5.2. Adjust the potentiometer to set the voltage gain to precisely –1. This circuit is a simple phase-splitter and is used to generate a differential input signal.

12. Connect the circuit of Figure 6.5.2 to the original circuit as shown.

13. Measure and record the output voltage in Table 6.7.3.

14. Based on the results of Table 6.7.3, compute the experimental common-mode rejection ratio and place it in Table 6.7.4.

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9.5.7: Data Tables

Theoretical Differential Gain	

Table 9.5.7.1

Input	V_{out}	Phase	A_v
V_{inv}			
V_{non}			

Table 9.5.7.1

Circuit	V_{out}	A_v
Superposition		
Common-mode		
Differential		

Table 9.5.7.1

Experimental CMRR	

Table 9.5.7.1

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9.5.8: Questions

1. What controls the differential gain?

2. Why is it important to match the resistor ratios in step 3?

3. Why is it important to set the gain of the phase-splitter to precisely one in step 11?

4. What determines the theoretical maximum CMRR for the op amp differential amplifier?

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